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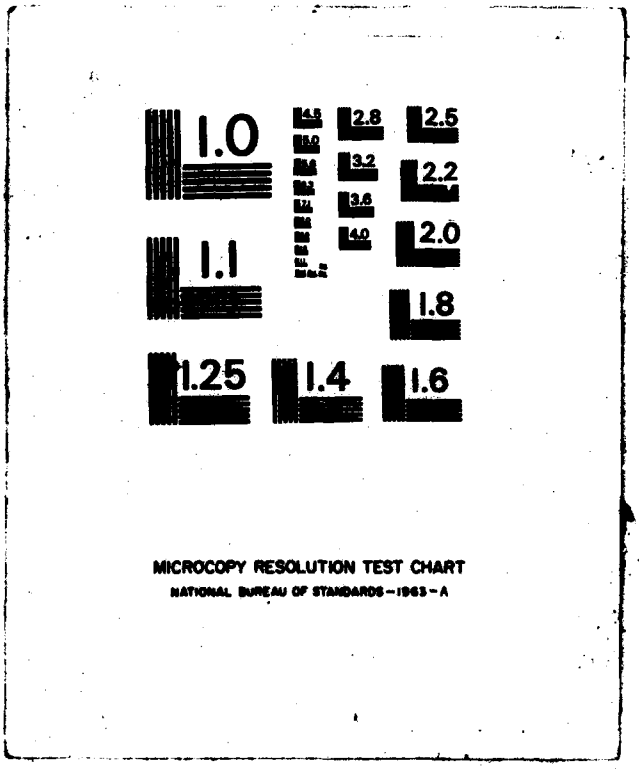
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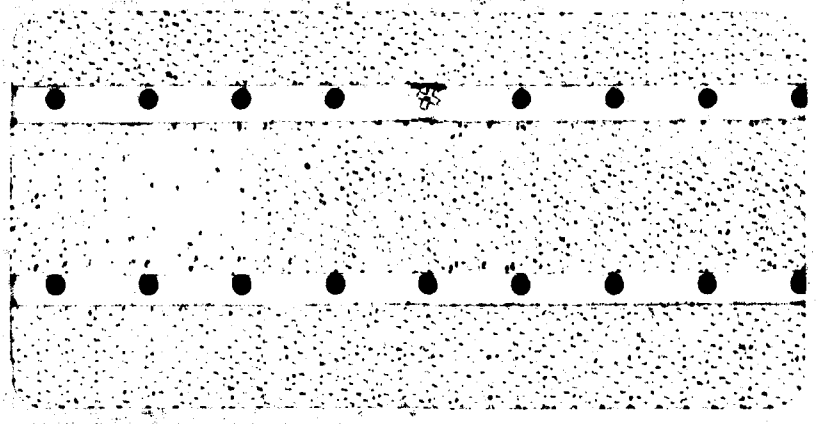

Electrical and Computer Engineering

University of Massachusetts
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Numerical Simulation of the Permeable Base Transistor

by

D. H. Navon and T. W. Tang

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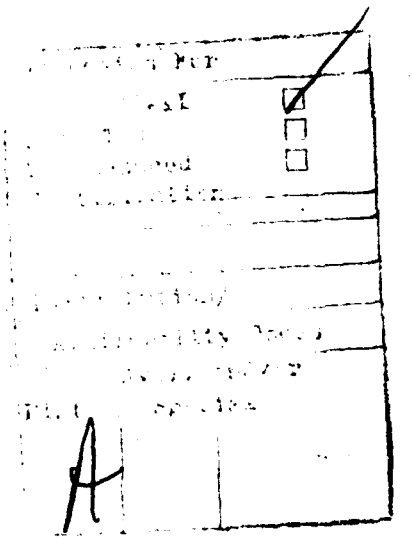
Predictions of improved high frequency performance of the gallium arsenide permeable base transistor (PBT) have been made by the exact diffusion-drift, two-dimensional numerical analysis of several PBT designs. In this study both the device geometry and/or the impurity doping profile were varied and the corresponding unity-current-gain frequency, f_T, calculated. More than a 35% improvement in f_T was predicted when the ratio of the metal (Schottky) gate width to the space between gate fingers was varied. More than a doubling of f_T could be otained when the source and drain doping was increased to produce an $n^+ n n^+$ configuration. Each device design was analyzed to determine the change in mobile charge density with gate bias in the major areas of the structure in order to compute its contribution to the device input capacitance. In this way information was obtained on design details for reduced capacitance and transconductance change for improved f_T. A new UPBT structure was investigated where the semiconductor material above the gate electrode was removed in order to reduce this region's contribution to the capacitance. A 100% improvement in high frequency performance was predicted for this structure, operating at low gate voltages. Less gain was obtained at higher voltages. Control of the surface states on the exposed "walls" of this device must be provided to obtain this advantage.



FINAL REPORT

on the

NUMERICAL SIMULATION OF THE PERMEABLE BASE TRANSISTOR

Research performed

1 April 1982 to 30 June 1982

by

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Abstract

Predictions of improved high frequency performance of the gallium arsenide permeable base transistor (PBT) have been made by the exact diffusion-drift, two-dimensional numerical analysis of several PBT designs. In this study both the device geometry and/or the impurity doping profile were varied and the corresponding unity-current-gain frequency, f_T, calculated. More than a 35% improvement in f_T was predicted when the ratio of the metal (Schottky) gate width to the space between gate fingers was varied. More than a doubling of f_T could be obtained when the source and drain doping was increased to produce an n^+ n n^+ configuration. Each device design was analyzed to determine the change in mobile charge density with gate bias in the major areas of the structure in order to compute its contribution to the device input capacitance. In this way information was obtained on design details for reduced capacitance and transconductance change for improved f_T. A new UPBT structure was investigated where the semiconductor material above the gate electrode was removed in order to reduce this region's contribution to the capacitance. A 100% improvement in high frequency performance was predicted for this structure, operating at low gate voltages. Less gain was obtained at higher voltages. Control of the surface states on the exposed "walls" of this device must be provided to obtain this advantage. A time-dependent analysis of PBT operation in a circuit environment is suggested in order to optimize the device design for switching and amplifier applications.

Table of Contents

I. Introduction

The Permeable Base Transistor was first reported at the Seventh Biennial Cornell Electrical Engineering Conference held in 1979 at Cornell University, Ithaca, NY as "A new transistor.....which may have a maximum frequency of oscillation greater than 1000 GHz", by a group of researchers at the MIT Lincoln Laboratory [1]. Advantages claimed for this device were that it is a majority carrier device like an FET, but also has the higher transconductance of a barrier controlled device like the BJT.

Subsequently a two-dimensional simulation of a GaAs permeable base transistor (PBT) was published by members of this same Lincoln Laboratory group [2]. They predicted a unity-gain-frequency, f_T = 88 GHz. and an f_{max} approaching 400 GHz for a device with a 0.2μm openings between gate fingers. A cross section of this device is shown sketched in Fig. 1a. The gate electrodes were assumed to be Schottky barriers. Also shown in this drawing are the boundary conditions assumed in their calculations.

More recently researchers at the Hughes Research Laboratories have published a numerical evaluations of the PBT for application in silicon integrated logic circuits [3]. They predict maximum unity-current-gain frequencies as high as 80 GHz as well as operating frequencies up to 30 GHz for a silicon logic inverter circuit. In their computations they studied the effect of the variation of gate finger thickness and finger spacing on f_T. Thinner gate metalization and closer finger spacing are predicted to yield higher f_T.

The objective of the presently reported research on the design aspects of the GaAs PBT is to evaluate the effect on the frequency behavior of the variations of device geometry and/or the impurity doping profile in the structure. This was done by obtaining an exact solution of the drift-diffusion equations in two-dimensions using numerical analysis. The general method used has previously been reported by our group [4]. In particular, the following tasks were performed to determine the effect of the variations in device design on the unity-current-gain, f_T:

1. The ratio of gate finger width to gate finger spacing, R, was varied, maintaining a fixed device chip size.
2. The contributions to the input capacitance of the various sectors of the device structure were determined.
3. The source and drain region doping was increased to create an n^+ n n^+ structure.
4. The semiconductor material above the gate electrodes was removed to simulate a device structure which could be more easily fabricated.

In each case, the complete I-V characteristics of output drain current versus input gate voltage was computed. In addition, the electric equipotentials and carrier density distribution in the device structure were generated. Finally, the frequency behavior was predicted by computing f_T versus gate voltage.

II. Method of Analysis

The electrical behavior of the gallium arsenide permeable base transistor was studied by obtaining the simultaneous steady-state solution in

two-dimensions of the Poisson charge equation for the electric potential and the current continuity equation. This yields the electric potential and electron carrier density everywhere in the device structure. These equations may be written respectively as:

$$\nabla^2 \psi = - \frac{q}{\varepsilon} (N-n) \tag{1}$$

and

$$\nabla \cdot \vec{J} = qR, \tag{2}$$

with the auxiliary equation

$$\vec{J} = - q\mu n \vec{\nabla}\psi + qD \vec{\nabla}n. \tag{3}$$

Here ψ is the electric potential, n is the electron carrier density, N is the net ionized impurity density, q is the electron charge, ε is the semiconductor dielectric constant, μ and D are the electron mobility and diffusion constants, respectively, and R is the carrier recombination rate which is taken here as zero since the PBT is assumed to be a majority carrier device. The mobility is assumed to be a piecewise linear function of the electric field as well as the impurity density [See Fig. 1b]. The Einstein relation providing a relationship between the mobility and diffusion constant is used.

It is assumed that the charge carriers are at all times in thermal equilibrium with the lattice and that the Boltzmann approximation of the Fermi statistics, expressed as:

$$n = n_i \exp \frac{q(\psi-\phi)}{kT}, \tag{4}$$

is valid. Here ϕ is the quasi-Fermi potential for electrons and n_i represents the intrinsic carrier density of the gallium arsenide.

The electrical equations are solved subject to the boundary conditions specified in Fig. 1a. Symmetry conditions at the right and left boundaries dictate that the gradients of ψ and ϕ normal to these boundaries are each zero. The source (or emitter) and drain (or collector) contacts are assumed to be ohmic so that the semiconductor material immediately adjacent is considered to contain the equilibrium density of electrons characteristic of the impurity concentration there. The gate (or base) electrode is assumed to be a Schottky contact with the potential in the adjacent material defined by the impurity density and barrier height as given in Fig. 1a. In the simulation of the device where the semiconductor material above the gate is removed, a free surface or wall is produced. The continuity of the tangential component of the electric field at the semiconductor - dielectric interface is used as well as the discontinuity of the normal component of the dielectric induction there due to a surface charge, Q_{ss}.

III. Numerical Solution Method

The differential equations (1) and (2) are first discretized and the resulting algebraic equations are written at every point of the nonuniform grid as shown in Fig. 2. These discretized nonlinear equations may be expressed in the matrix form

$$FX = b, \tag{5}$$

where X is the solution vector containing the unknown variables $\psi_{i,j}$ and $\phi_{i,j}$, where i varies from 1 to N and j from 1 to M, covering all the grid nodes. F is the nonlinear operator representing the controlling equations and b is the known vector representing the known parameters and boundary conditions of the operating structure analyzed. Now Newton's method is

used which in effect reduces this nonlinear problem to the solution of a set of linear equations. Newton's method is an iterative procedure which, when an approximate solution is assumed, a successively better approximation is obtained by solving a linear approximation to the nonlinear problem. If vector G(X) is defined as

$$G(X) = FX - b, \tag{6}$$

the solution of this equation, X*, is such that G(X*) = 0. Assuming an approximate solution say X_k, then a better approximation to X* is achieved by solving the linear equations

$$A\delta = a, \tag{7}$$

where A is the Jacobian matrix of G evaluated at X_k and a is $-G(X_k)$. This gives the correction vector δ_k such that

$$X_{k+1} = X_k + \delta_k. \tag{8}$$

This procedure is repeated as often as necessary until the solution is achieved to a preset accuracy. The inversion of the matrix A is often impractical and hence is normally carried out by the indirect method of successive line overrelaxation [SLOR].

IV. Results

The procedure followed in this research was to solve equations (1) and (2), coupled with equation (3), for ψ the electric potential and ϕ the quasi-Fermi potential (which yields the electron carrier density, n) at every node in the device grid structure. This was done for various values of gate potential, V_G, with the value of drain voltage, V_D, held fixed at 1.0 volts. Now the drain current was calculated for each value of V_G so that an entire transfer characteristic could be calculated. The unity-current-gain, f_T, was computed from the expression

$$f_T = \frac{g_m}{2\pi C_{in}} , \tag{9}$$

where $g_m \equiv [\partial i_d/\partial v_g]_{v_d}$ is the transconductance obtained by calculating the change in drain current for an incremental change in gate voltage, at a fixed value of drain potential; $C_{in} \equiv [\partial q_m/\partial v_g]_{v_d}$ is the input capacitance obtained by calculating the change in total integrated mobile charge in the device for an incremental change in gate voltage at a fixed drain potential.

A. Gate Width Variation

An investigation was made on varying the ratio of the gate width, 2d, to the distance between gate fingers, keeping the center-to-center spacing between gate fingers (and hence the device, or chip size) constant. The results of these calculations are shown in Figs. 3-7. Fig. 3 gives a plot of the equipotential lines, in the device segment pictured, with a drain potential of 1.0 volts, a gate potential of 0.6 volts, and with the ratio of the gate width to spacing between gate fingers, R = 0.25. Only a segment of the device was analyzed since by symmetry considerations the entire device operation may be reconstructed by repeating this element. The dimensions of this device segment was taken as 0.20μm x 1.0μm, as originally reported by the Lincoln Laboratory group [1].

Fig. 4 shows the corresponding plot of equi-electron density lines for the same device segment. The donor doping in the GaAs bulk material is taken as $1 \times 10^{16}/cm^3$. This corresponds to an equi-concentration contour marked n = 1.0 in Fig. 4; this figure indicates electron carrier depletion near the gate electrode (n<1.0) and accumulation (n>1.0) near the center-line between gates.

Fig. 5 is a plot of the output drain current per cm. finger length versus input gate voltage. Shown are 3 graphs representing the gate width factors, R = 0.25, 0.4, and 0.6. This increase in drain current as, R, and the gate width decrease, gives rise to improved f_T with the narrowing of the gate fingers. Of course if the gate thickness, L, is maintained constant, this would represent a decrease in gate metallization cross-section and hence increased gate series resistance. This could limit the operating gain of the device at high frequencies. Finally Fig. 6 gives a plot of f_T versus gate voltage for 3 different values of R. Again finger narrowing means improved f_T.

Fig. 7a and 7b show the operating device current streamlines following from drain to source. The mode of operation of the PBT normally requires that under zero bias conditions that the built-in Shottky barrier space-charge region pinches off the conducting channel region. Then the application of forward gate bias (gate positive with respect to source) lowers the barrier, permitting substantial current to flow. In Fig. 7a the gate bias is only 0.3 volts, and hence the current is constrained to flow through a narrow channel opening. In Fig. 7b the Schottky space-charge region is even more decreased by the application of higher forward gate bias, 0.6 volts, so that the channel current flow is less constricted.

B. Contributions to the Input Capacitance

An investigation was made in order to determine the contribution of each of the various segments of the PBT device structure on the input capacitance. The device was divided up into 3 parts: section 1 extends the full length of the device and occupies the channel region, between gate fingers, as shown in Fig. 8. Section 2 is the region above the gate

electrode, near the source; section 3 is the region below the gate near the drain. A numerical analysis was made to determine the input capacitance contribution from each of these segments by integrating the mobile charge change due to an incremental change in gate voltage. As seen in Fig. 8, sector 1 makes the largest (50%) contribution to the input capacitance. Due to charge accumulation in the channel region at higher gate voltages there is a tendency for the capacitance contribution of section 1 to increase with gate potential, but then level off. At even higher gate voltages some of this charge moves into the drain region, section 3, with a corresponding drop in the sector 1 contribution.

C. Impurity Doping Profile Variation

Since most of the electrically active region of the PBT is near the gate electrode, it seemed advisable to increase the doping level near the source and drain region to concentrate the controlling field near the gate Schottky barrier as well as minimize series source and drain resistance. PBT devices with doping profiles of this type, sketched in Fig. 9, were investigated and found to give improved high frequency possibilities. N^+ n n^+ structure devices were modeled with a middle region n-doping of $1 \times 10^{16}/cm^3$ and a source and drain region maximum surface doping of up to $1.25 \times 10^{17}/cm^3$.

Fig. 10 gives the calculated transfer characteristics of these new designs. Here the output drain current is computed as a function of input gate voltage, for 3 different doping profiles.

1. uniform doping of 1×10^{16} donors/cm^3
2. increased source/drain maximum surface doping of $6 \times 10^{16}/cm^3$
3. source/drain maximum doping of $1.25 \times 10^{17}/cm^3$.

Increased output drain current is predicted as the source/drain doping is successively increased above the original, uniform doping. However the percentage improvement is much more pronounced at lower gate voltages than at higher values of gate voltage and hence high drain current.

A significant increase in f_T was also predicted for the case of increased source and drain region doping. This is shown in Fig. 11. At a gate voltage of about 0.3 volts, nearly a doubling of f_T was calculated for the case of heavy source/drain doping compared to the uniform, $1 \times 10^{16}/cm^3$ impurity doped device. However at about 0.5 gate volts this improvement was reduced to 40%.

In order to investigate the basis of this improvement in frequency response, both the g_m and input capacitance were examined as a function of gate voltage, since both these factors determine f_T (see Eq. (9)). Fig. 12 shows the variation of the transconductance with gate voltage. This is obtained by calculating the incremental change in drain current for a small change in gate voltage, at a given value of drain voltage. Significant improvement in g_m, more than a doubling, is found at 0.3 gate volts, whereas only a 60% gain is predicted at a gate voltage of 0.5 volts for the case of the more heavily doped source and drain regions compared to the uniformly doped case. The input capacitance is computed by noting the increment in integrated mobile charge in the device for a small change in gate voltage. Here the input capacitance is seen to increase as the source/drain doping is increased. This tends to offset the improvement in frequency behavior obtained by the increase in g_m. However at gate voltages of both 0.3 volts and 0.5 volts only a 20% increase in input capacitance over the uniformly doped case is calculated. These results are shown in Fig. 13.

These preliminary results on the device doping profile variation indicate that the optimum donor inpurity distribution has not as yet

been determined. It appears that an n^+ i n^+ structure should be best. However two and even three-dimensional doping profiles may be necessary to optimize the high frequency performance of the PBT. More heavily doped source/drain regions give rise to significantly improved g_m with marginal deterioration in the input capacitance. The gate to drain (Miller) capacitance should be minimized. Decreased doping in the channel, adjacent to the gate electrode should increase the rate of space-charge region reduction with increased gate voltage, at higher gate voltages. This may make more gradual the tendency of the g_m to saturate at higher gate potentials. Plots of electric potential and carrier density for these more heavily doped designs are shown in Figs. 14-19.

D. Removal of GaAs Material Above the Gate (the UPBT)

For reasons of ease of fabrication, it has been suggested that the GaAs semiconductor crystal material above the gate electrode be eliminated. This new device structure is sketched in Fig. 20. Here the indicated dielectric material which replaces the removed GaAs semiconductor was assumed to be an insulator with dielectric constant equal to 1.5, for the purpose of this calculation. The boundary conditions assumed are indicated in the figure.

It is expected that for fabrication the GaAs crystal would be grooved out first and then the gate electrode metallization subsequently deposited. This "trench-like" structure will be referred to hence forth as a U-groove permeable base transistor or UPBT. Improved high frequency performance may be expected from this new device structure since removal of source region material will reduce the input capacitance. The contribution to the capacitance of this region was computed previously in Section IV B (see Fig. 8). The transconductance, g_m, may also be improved. Hence according to Eq. (9), f_T should increase.

In order to analyze the UPBT structure of Fig. 20, an assumption must be made as to the nature of the vertical sourface or "wall" formed in creating the grooved-out structure. Since no current flows through that surface, $\partial\phi/\partial x = 0$, there. If no charge is present on this surface, then $\varepsilon(\partial\psi/\partial\psi)$ must be continuous across this boundary. However, if a uniform surface charge density, Q_{ss}, is assumed, then the dielectric induction must be discontinuous by this amount, across the boundary.

Calculations were carried out for the UPBT structure of Fig. 20 for $Q_{ss} = 0$ and for $Q_{ss}<0$. The value of N_{ss} $(=-Q_{ss}/q)$ was taken both as $10^{11}/cm^2$ and zero. The drain output characteristics that were calculated are shown in Fig. 21. Here the results of the calculations on the trench-like structure are compared with the conventional PBT, uniformly - doped design. Indeed improved gain is indicated for the case of $Q_{ss} = 0$; however no change is predicted for $N_{ss} = 10^{11}/cm^2$ at gate voltages below 0.3 volts. In fact deterioration of the device performance is predicted for this negative surface charge density at higher gate voltages. The corresponding effect on f_T is indicated in Fig. 22, predicting a doubling of the unity-current-gain at 0.3 gate volts and a 30% improvement of f_T at 0.5 volts, for $Q_{ss} = 0$. For $N_{ss} = 10^{11}/cm^2$, 25% improvement in predicted at 0.3 gate volts, with a negligible change at 0.5 volts.

The contributing factors to this high frequency gain improvement are indicated in Figs. 23 and 24. In Fig. 23 the g_m is shown to nearly double at 0.3 volts gate potential, when $Q_{ss} = 0$, with no improvement indicated at 0.5 gate volts. In Fig. 24, no change in input capacitance is calculated for $Q_{ss} = 0$ and 0.3 gate volts, but about a 30% reduction in capacitance is predicted at 0.5 volts, V_G.

The transconductance improvement results from the presence of the lower dielectric constant material in the trench above the gate electrode (see Fig. 20). Since no charges are present in this material, the Schottky barrier space-charge region can now only extend into the channel region plus the area below the gate electrode. Hence the barrier height in the channel region, for a given gate potential is altered by the trench and g_m improvement results. Similarly the capacitance reduction at 0.5 gate volts is due to the lower dielectric constant of the trench material, and is illustrated in Fig. 24.

An even greater decrease in input capacitance is computed in the case of $Q_{ss}<0$, but this results in only marginal f_T improvement since some reduction in g_m occurs. This reduction in capacitance for $Q_{ss}<0$ results from the formation of an ionized donor depletion layer which is induced by Q_{ss} and fills a substantial portion of the source region near the vertical wall (see Fig. 20). This constricts the current flow and hence deteriorates g_m.

Some additional insight into the factors that control the input capacitance of the PBT can be obtained by examining Fig. 25 for the non-uniformly doped device. Here the device structure is broken up into 4 sections, as shown. Section 1 is nearest the drain contact, and section 2 is on the drain side, below the gate electrode. Section 3 is just above the gate electrode on the source side, and section 4 is adjacent to the source contact. At gate potentials in excess of 0.2 volts, the capacitance is dominated by charges in regions 3 and 2, adjoining the gate electrode. The regions adjacent to the source and drain contacts are only important at very low gate voltages.

Additional insight into the UPBT operation can be obtained by examining the electric potential and carrier density plots for this device with $Q_{ss} = 0$ and negative Q_{ss} ($N_{ss} = 10^{11}/cm^2$), shown in Figs. 26-33.

V. Conclusions

The standard GaAs permeable base transistor (PBT) structure was analyzed using numerical techniques in order to predict the high frequency performance of this device. The device geometry was altered by changing the ratio of the gate electrode finger width to the gate finger spacing, keeping a fixed device chip size. The narrow finger device gave marginally improved gain. The contributions of the different sections of the device structure to the input capacitance of the PBT were calculated. At the higher gate potentials (above 0.2 volts) the regions surrounding the gate electrode dominated the capacitance. Increasing the impurity concentration near the source and drain electrodes was seen to improve f_T due to increased g_m, in spite of a small increase in input capacitance. Removing the semiconductor material above the gate electrode was found to increase f_T, particularly if the surface charges on the trench wall could be minimized. This was mainly caused by an increase in g_m, although some reduction in input capacitance was also computed. A complete steady-state electrical characteristic was calculated in 400 - 500 seconds on the UMASS CDC Cyber 175 computer.

VI. Suggestions for Additional Research

The short (3 month) research program reported above has generated sufficiently interesting results to call for additional research on optimum PBT design. This device structure lends itself to good high frequency behavior. In fact the low stray capacitance of this structure plus the possibility of achieving the saturated carrier velocity or greater (overshoot), over most of the transit distance through the device, bodes well for optimum high frequency performance [5]. Ballistic transport may be achievable with appropriate device design. The simplicity of this device structure leads itself well to reproducible high volume production.

Hence an optimization in device geometry and impurity doping profile should be sought.

This can be best achieved by a detailed numerical simulation of the device. The preliminary results reported herein give evidence that only an exact numerical calculation will yield the kind of unexpected results reported in this preliminary work. The numerical methods developed in this research are efficient and precise enough to make possible a detailed design optimization of this high frequency amplifier and switch [3].

The present study utilized the steady-state solution of the transport equations to yield small-signal circuit model elements to simulate the PBTs high frequency performance. By taking small changes in gate voltages, the corresponding increments in drain current and total mobile charge in the device permitted the calculation of the g_m and input capacitance, respectively. Only the f_T, was calculated; this as a figure of merit, in order to compare designs. What is also needed is the gain at a given operating frequency. This can also be obtained by generating a more detailed circuit model for the device from the steady-state solution. However this would be a small-signal calculation. In order to predict the large signal performance of the device in a circuit configuration, a time-dependent solution of the transport equations plus a coupling to the circuit equations is needed. This has previously been reported by our group for a BJT [6]. This computation would also permit the evaluation of the PBT as a large signal, high speed switch as well as for logic switching applications.

Finally a Monte Carlo carrier transport calculation would allow the investigation of design possibilities which might permit utilization of overshoot velocity transport, and hence even higher frequency performance.

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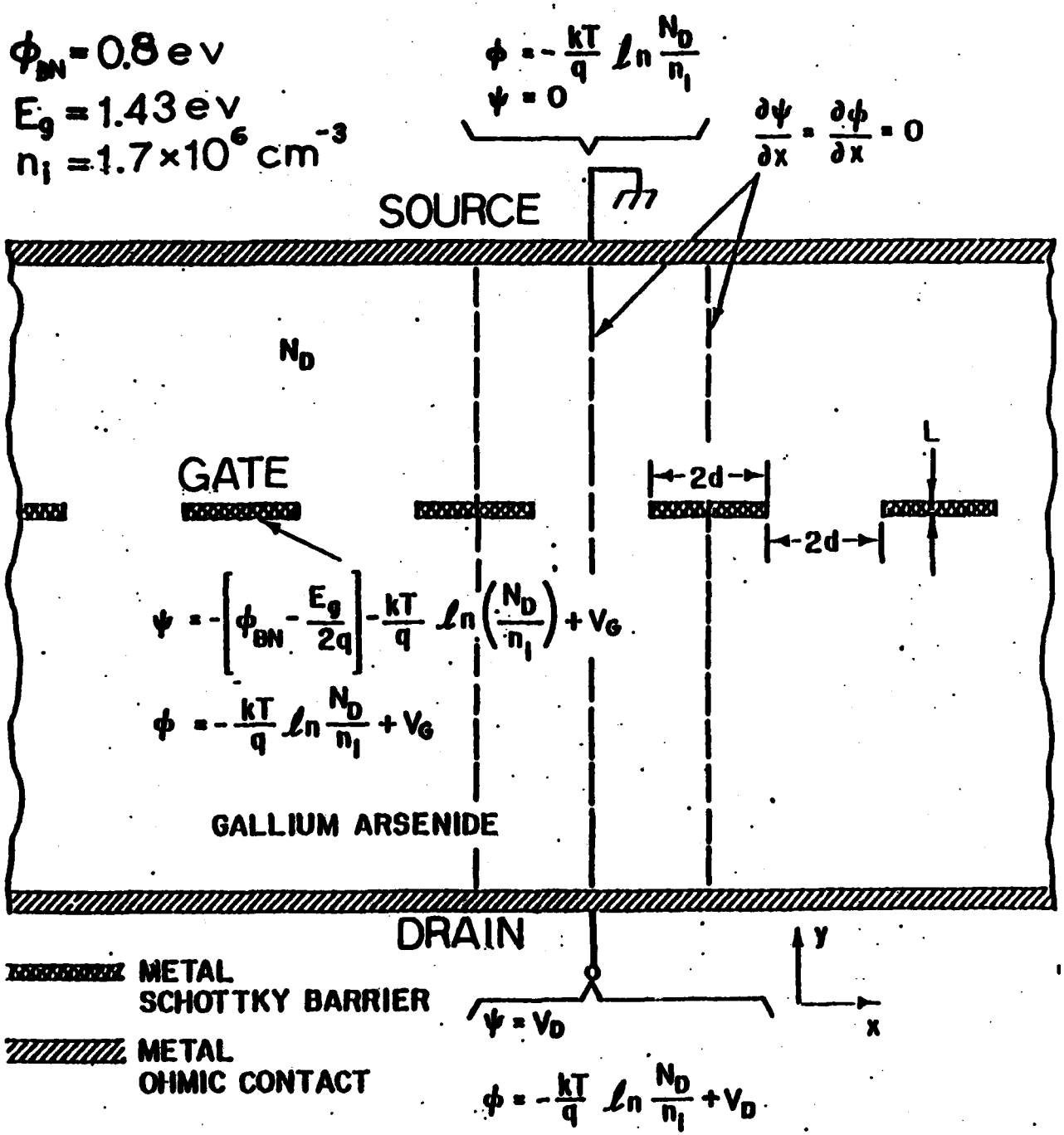


Fig. 1 a. The device geometry used in the numerical analysis showing a unit cell within the dotted lines and the boundary conditions.

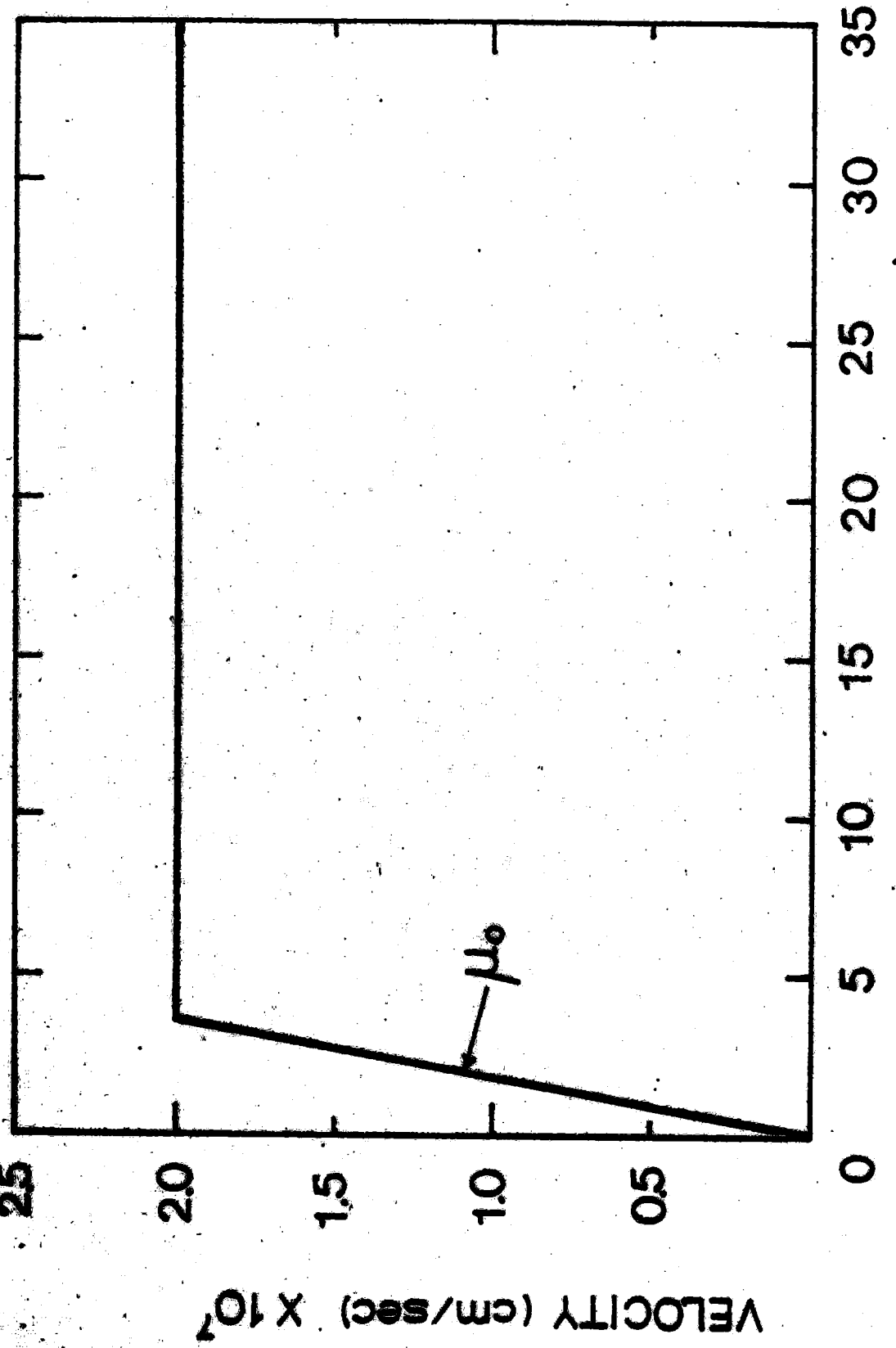


Fig. 1b. Velocity-field characteristic used in modeling PBT.

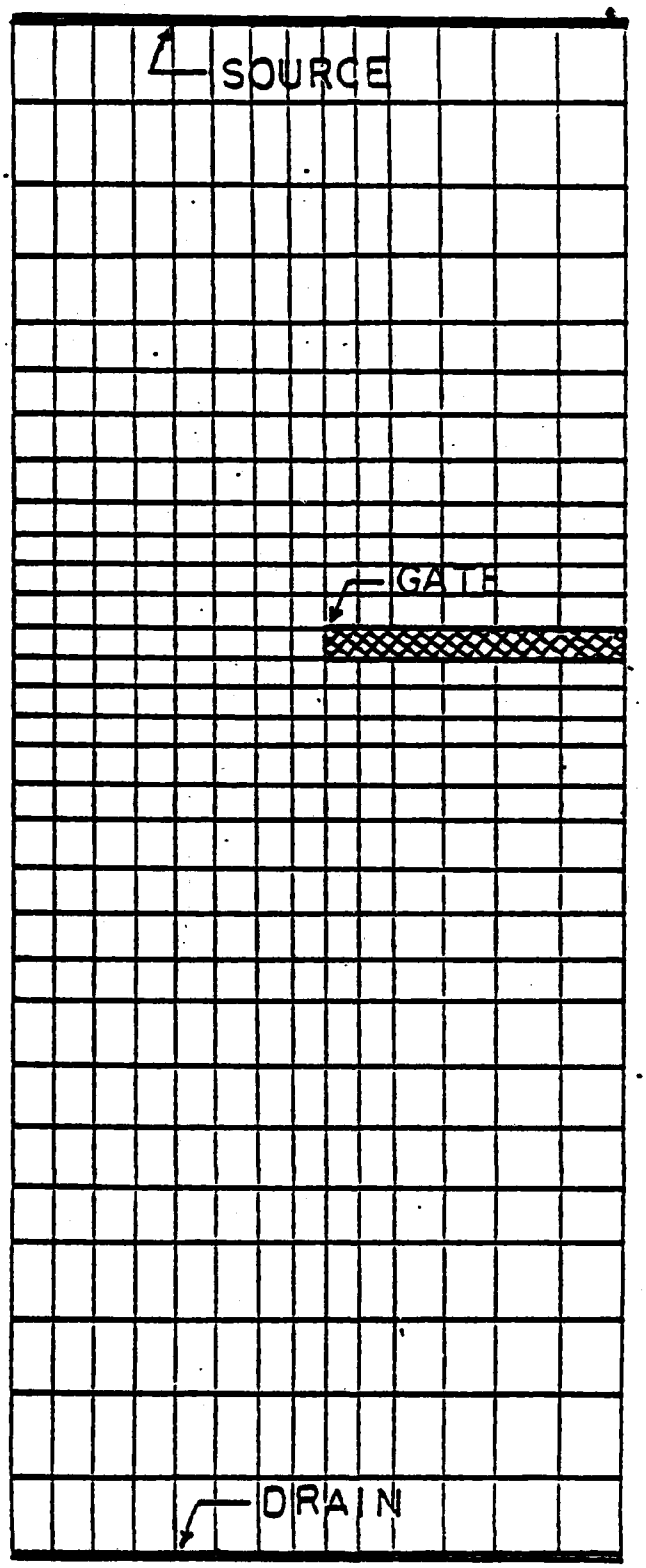


Fig. 2 Nonuniform grid structure

EQUIPOTENTIAL LINES (R = .25)

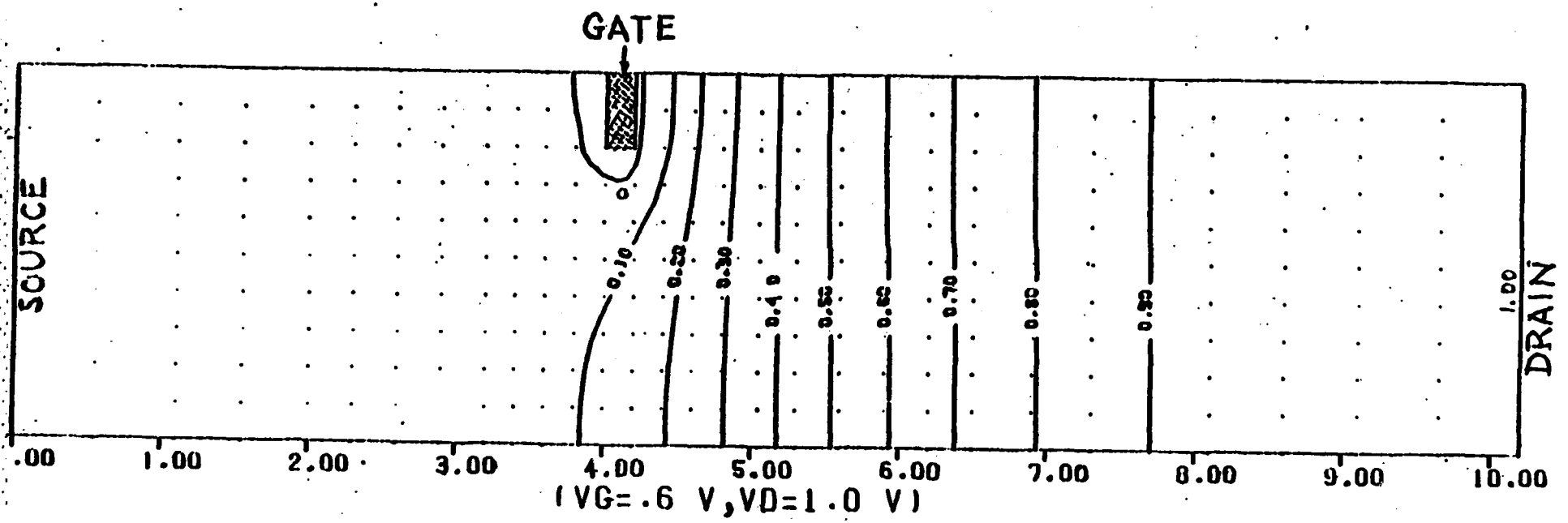


Figure 3

EQUI-ELECTRON CONCENTRATION LINES R=.25

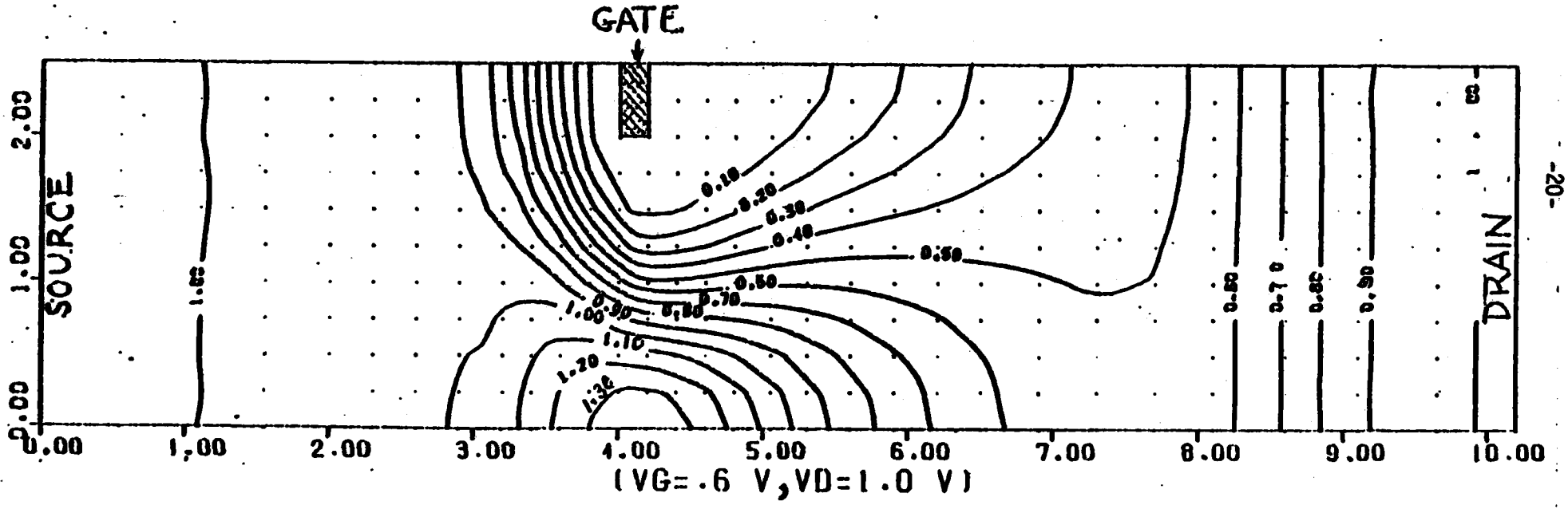


Figure 4

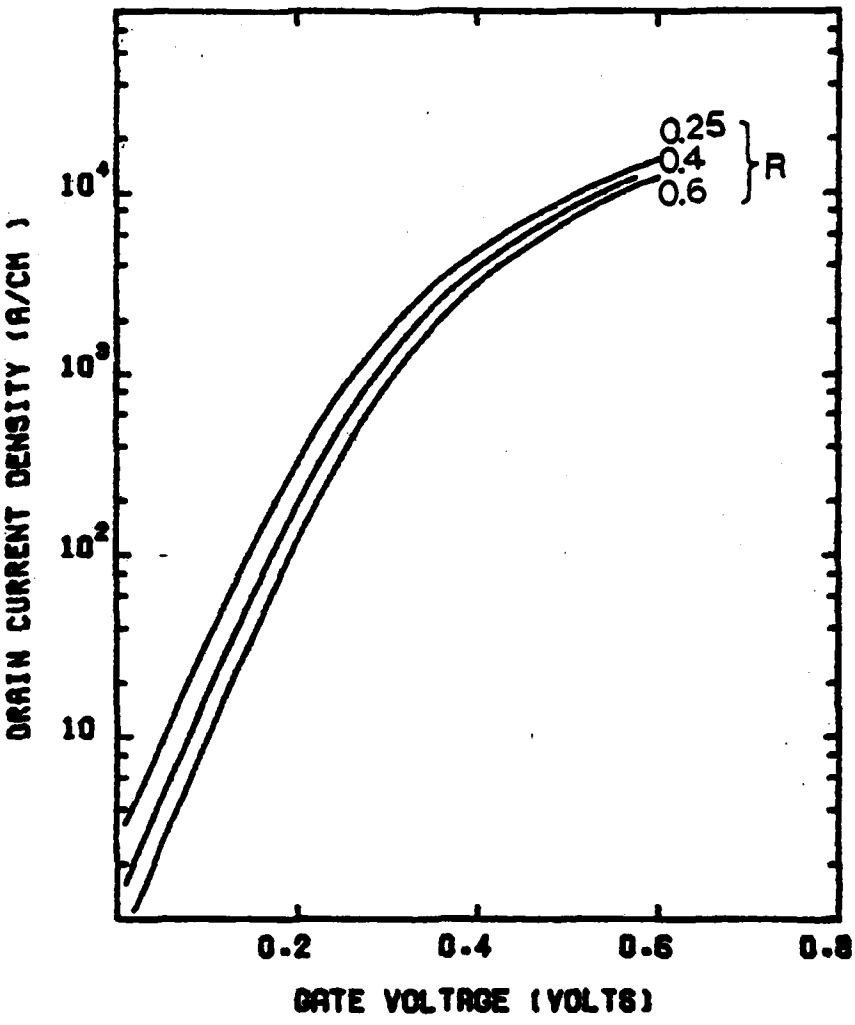


Fig. 5 Drain current density vs gate voltage

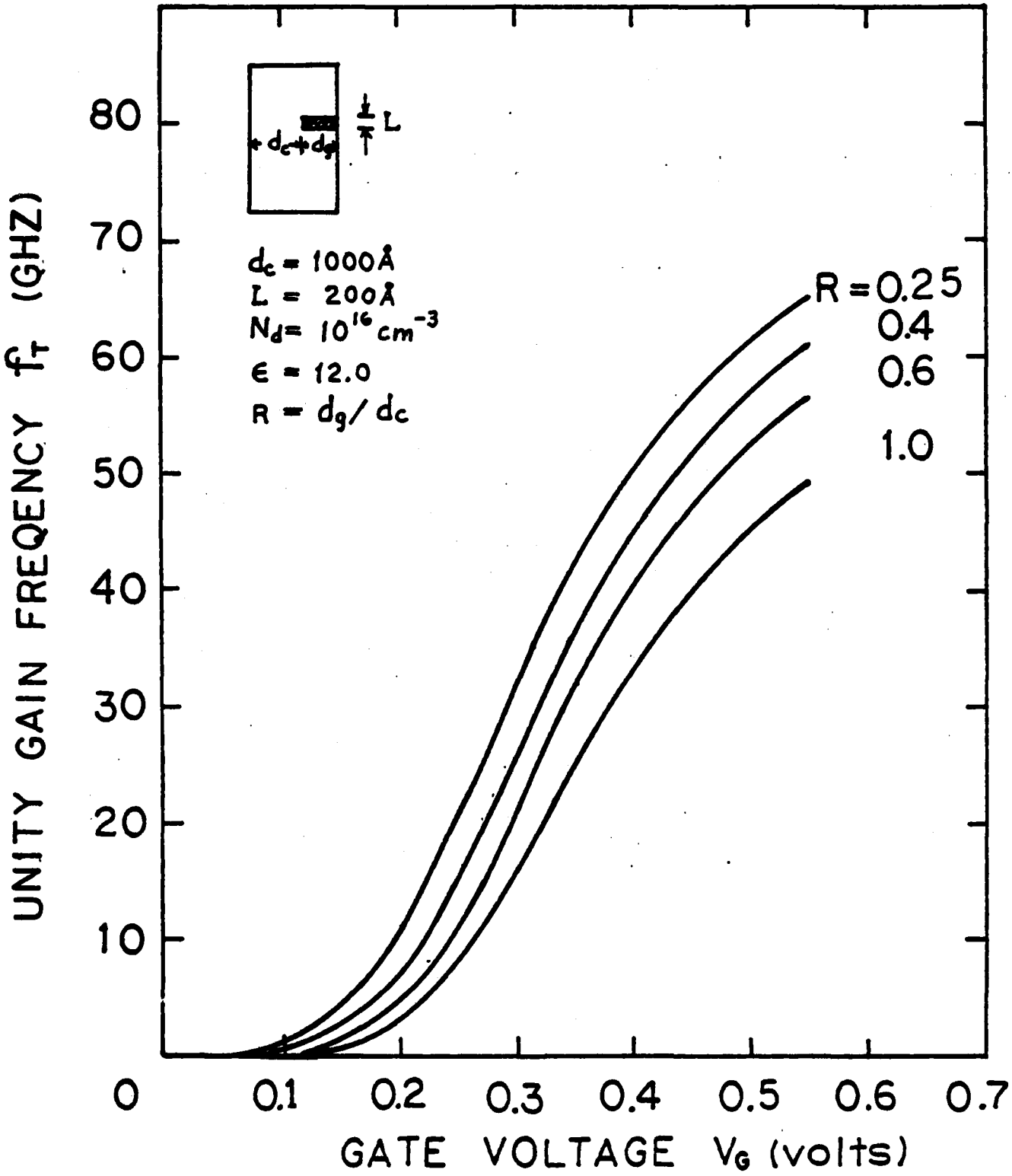


Fig. 6 Unity-current-gain frequency vs gate voltage

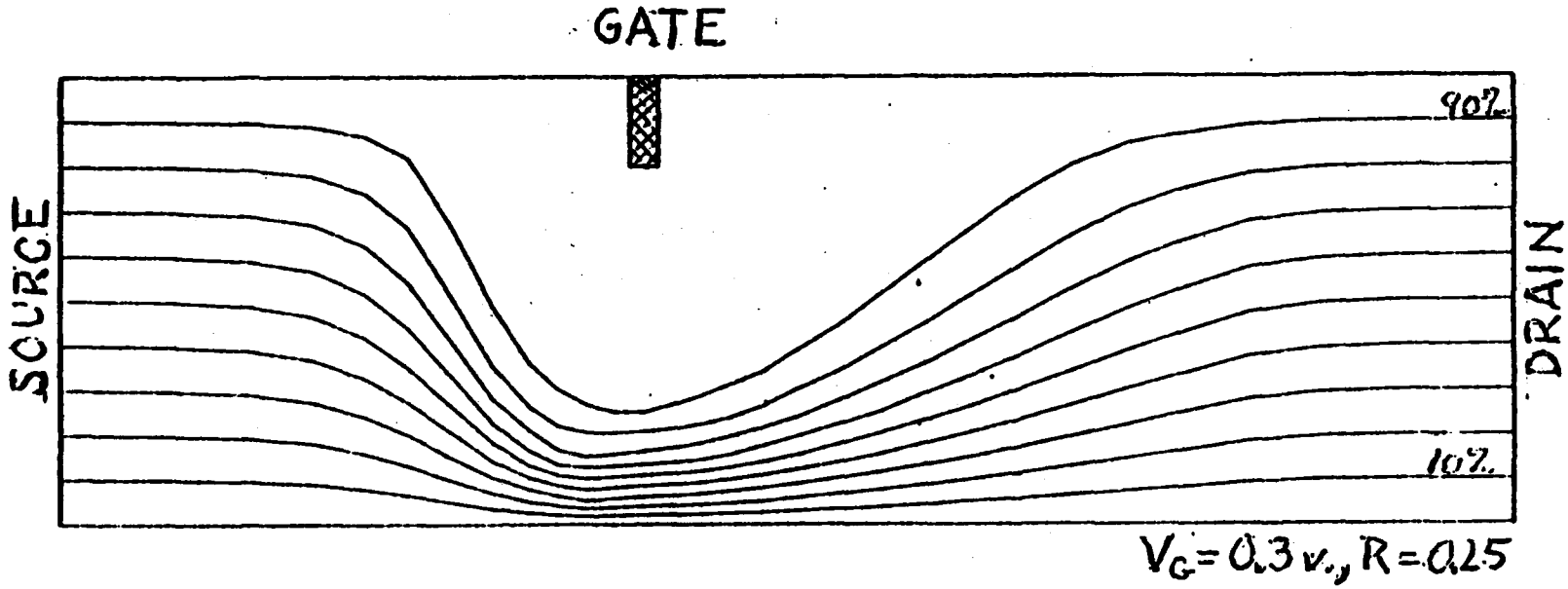


Figure 7a. Electron Current Distribution

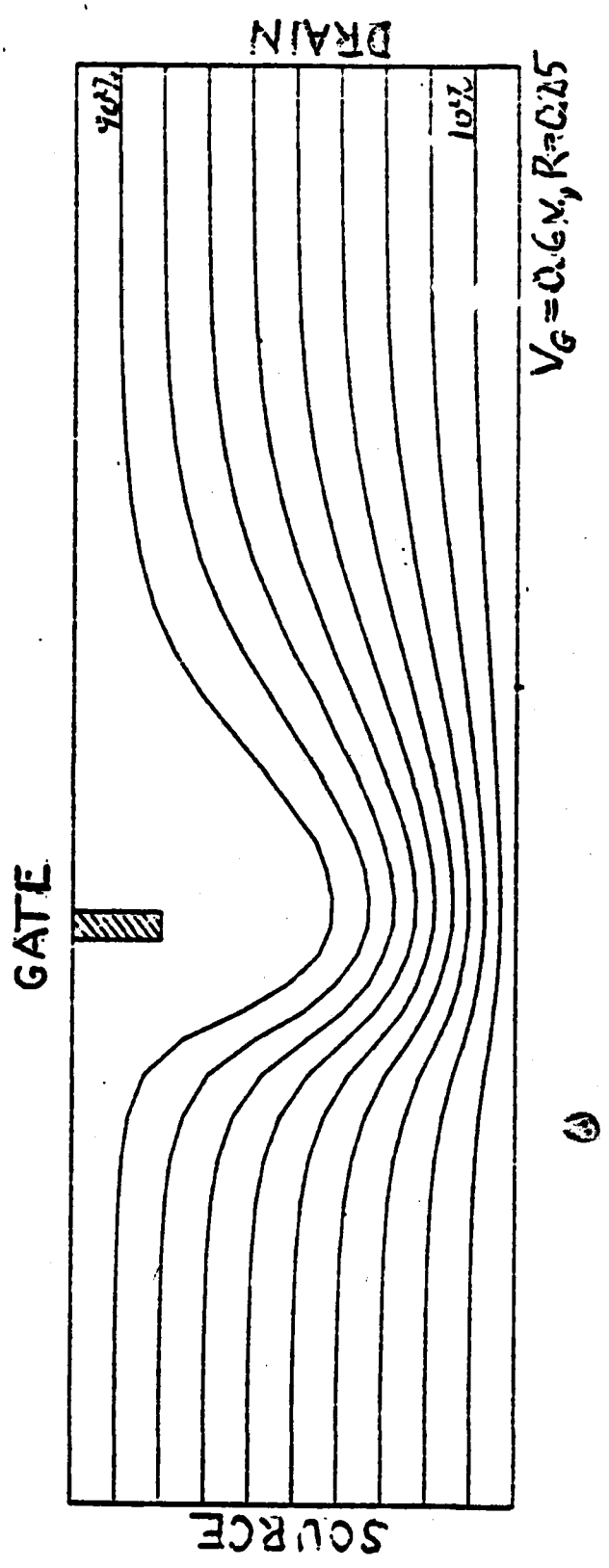
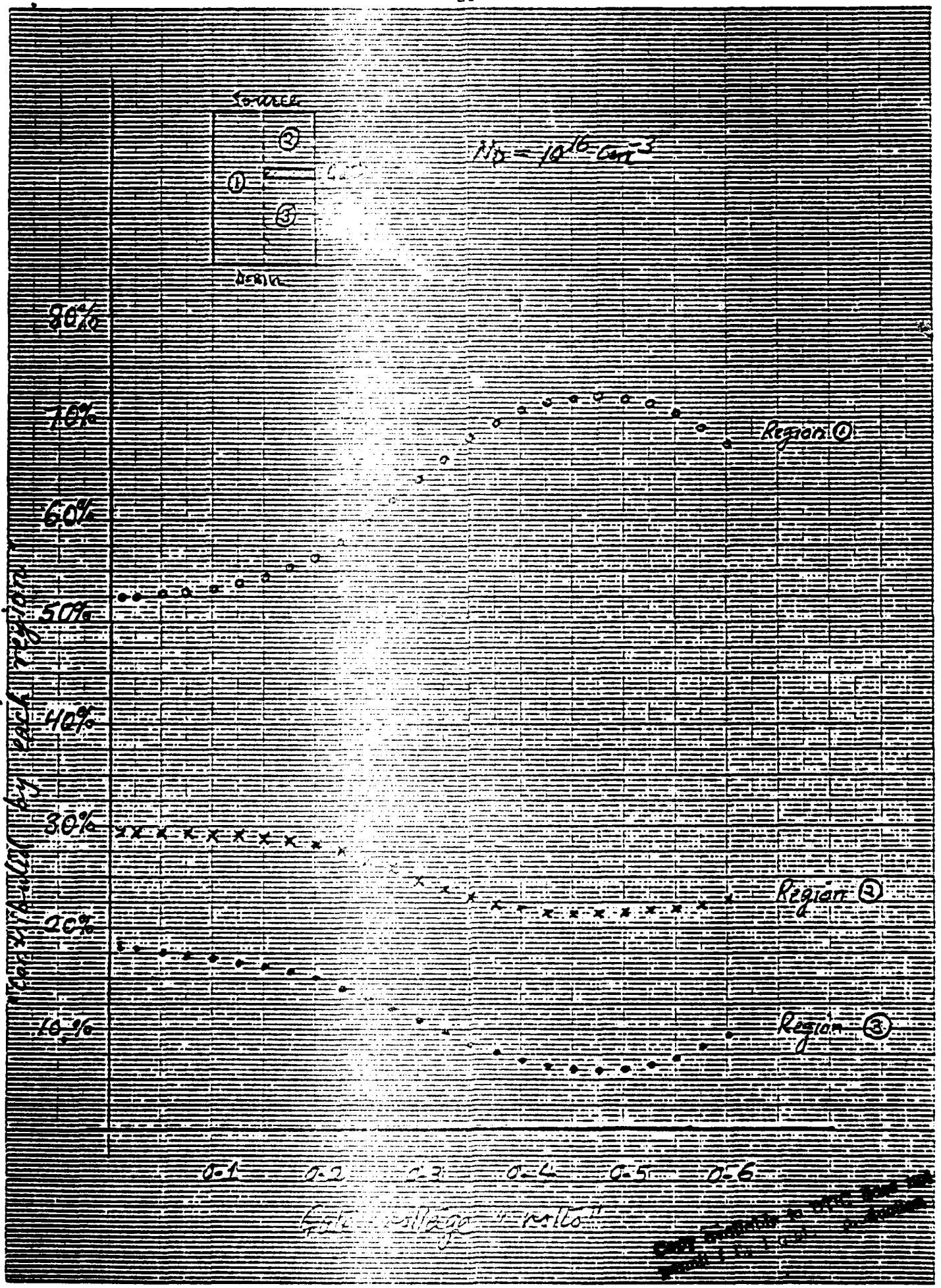


Figure 7b. Electron Current Distribution


Source
1
2
3
Drain
$N_D = 10^{16}\ cm^{-3}$
80%
70%
60%
50%
40%
30%
20%
10%
% of Total Capacitance Modulated by Each Region
Region 1
Region 2
Region 3
0-1
0-2
0-3
0-4
0-5
0-6
Gate Voltage (volts)

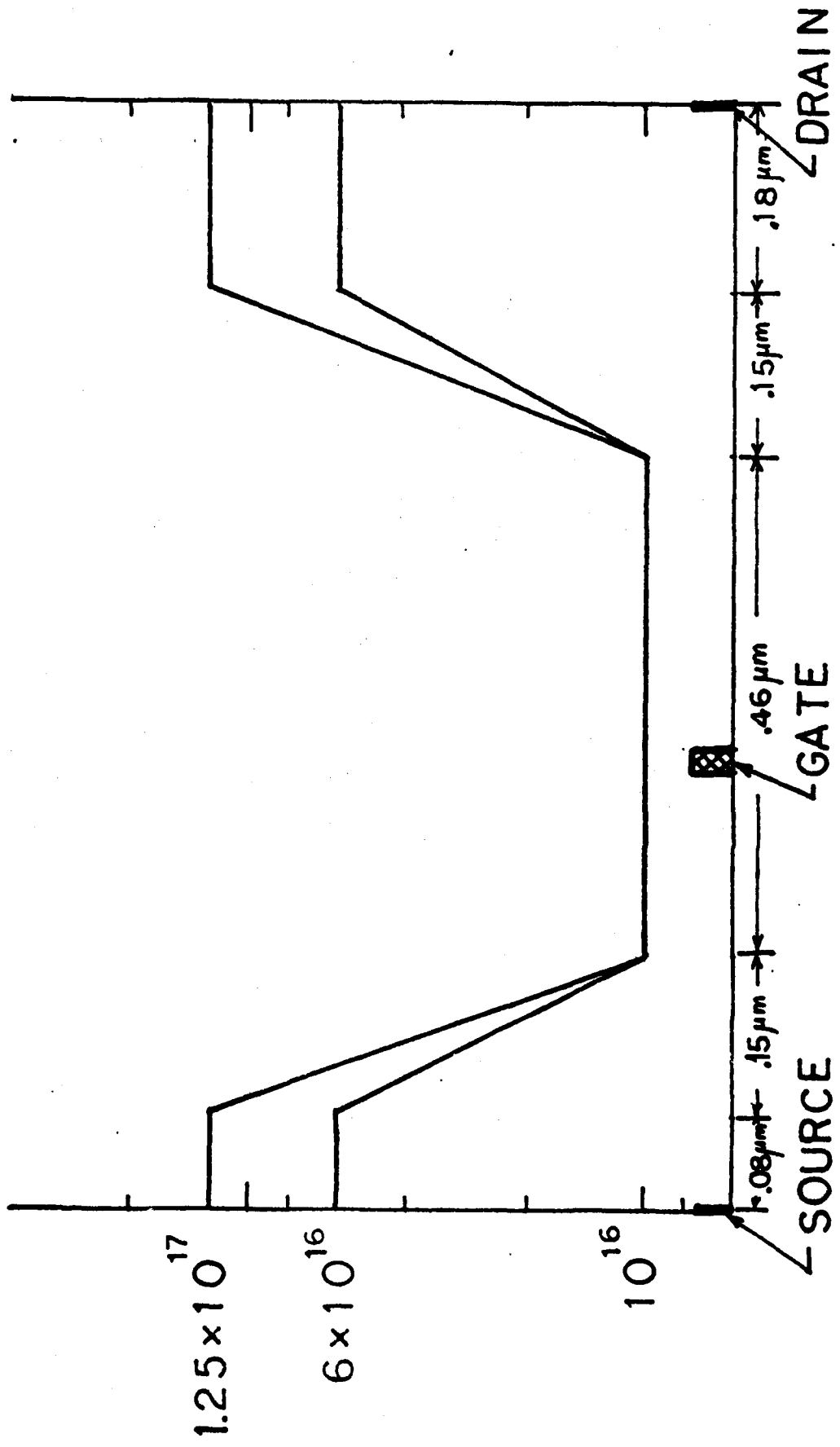


Fig. 9 Doping Profile along one grid line from source to drain.

Figure 10

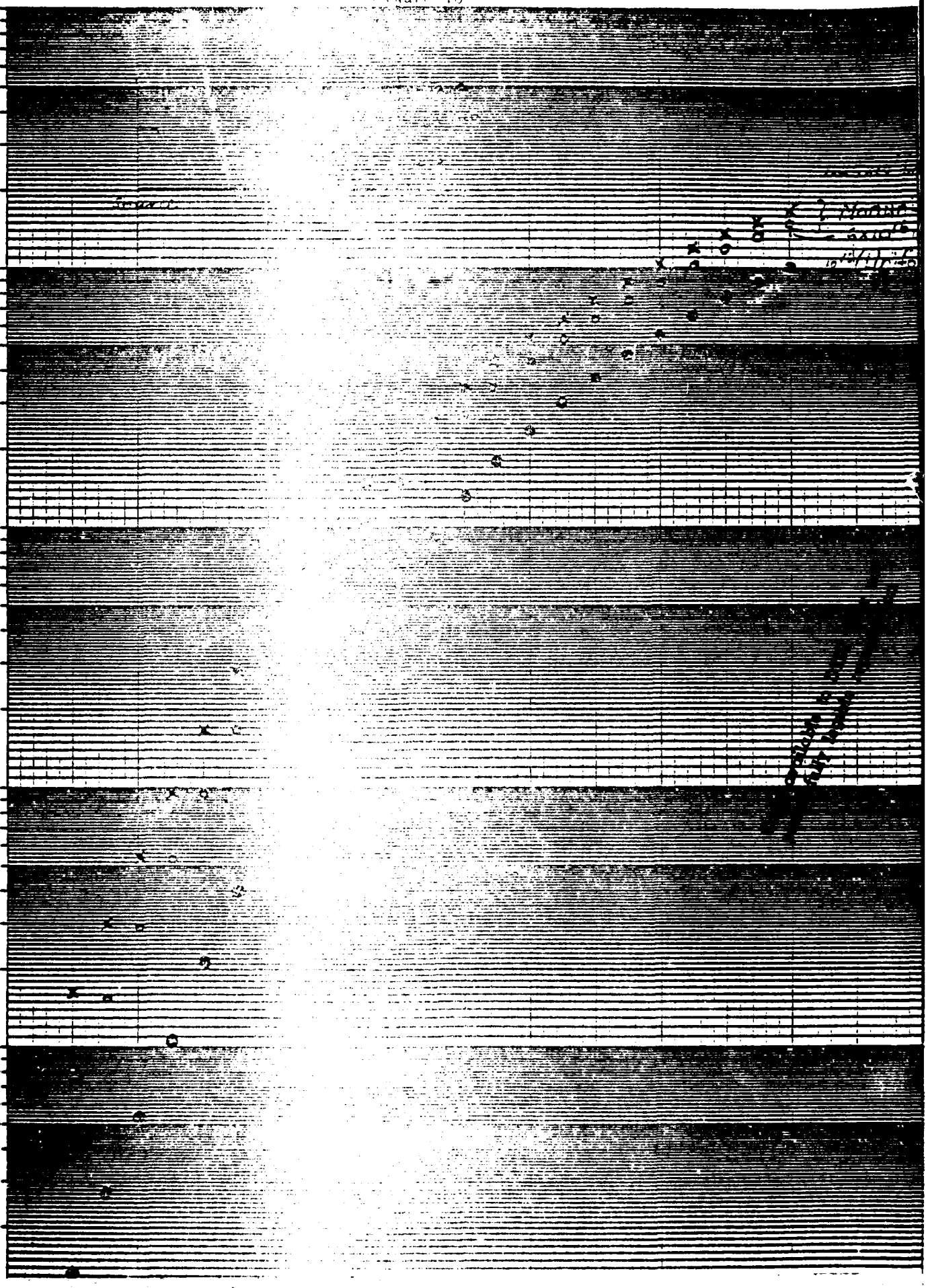


Figure 11

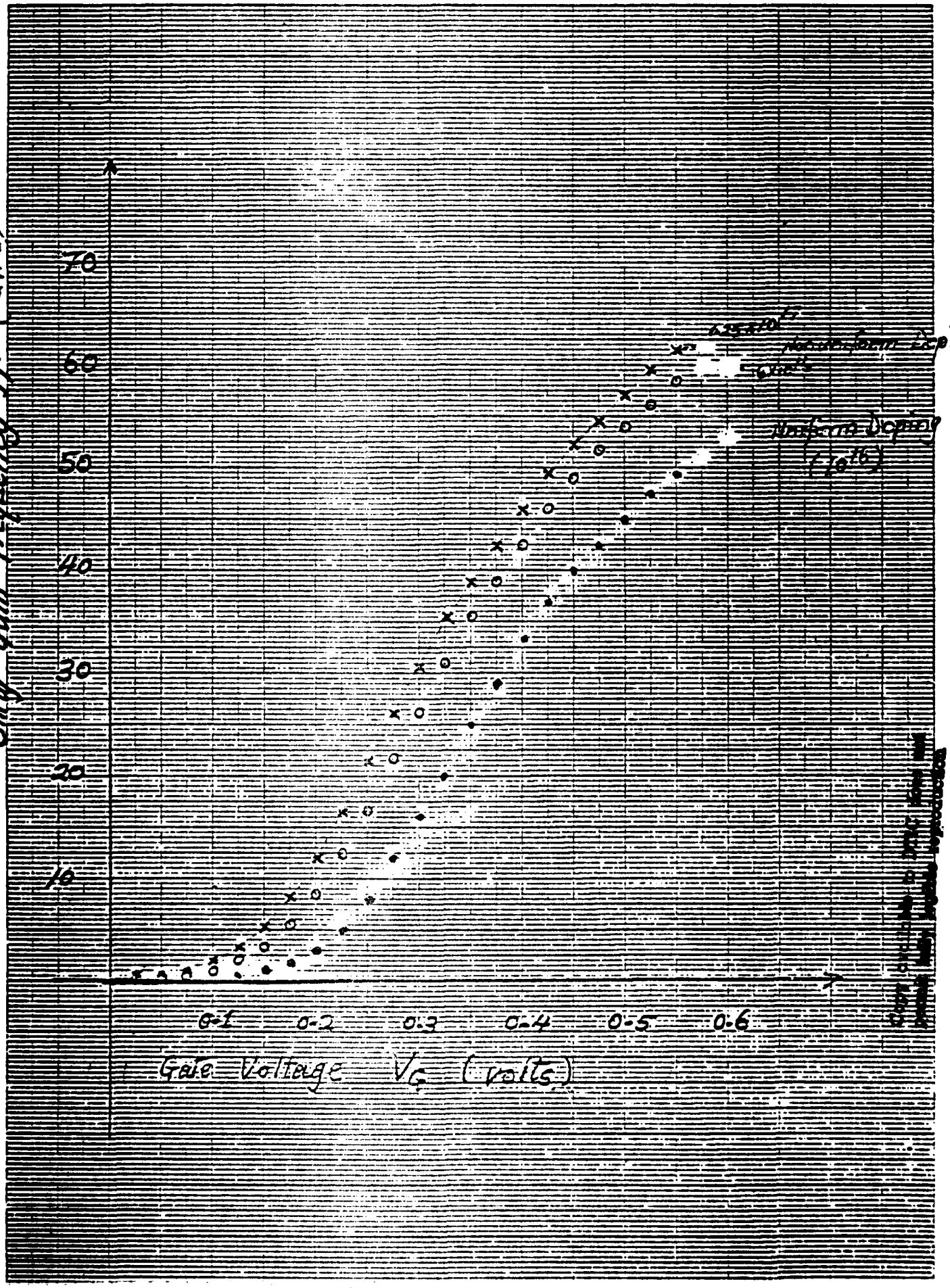

Unity Gain frequency f_T (GHz)
70
60
50
40
30
20
10
0·1
0·2
0·3
0·4
0·5
0·6
Gate Voltage V_G (volts)

Figure 12

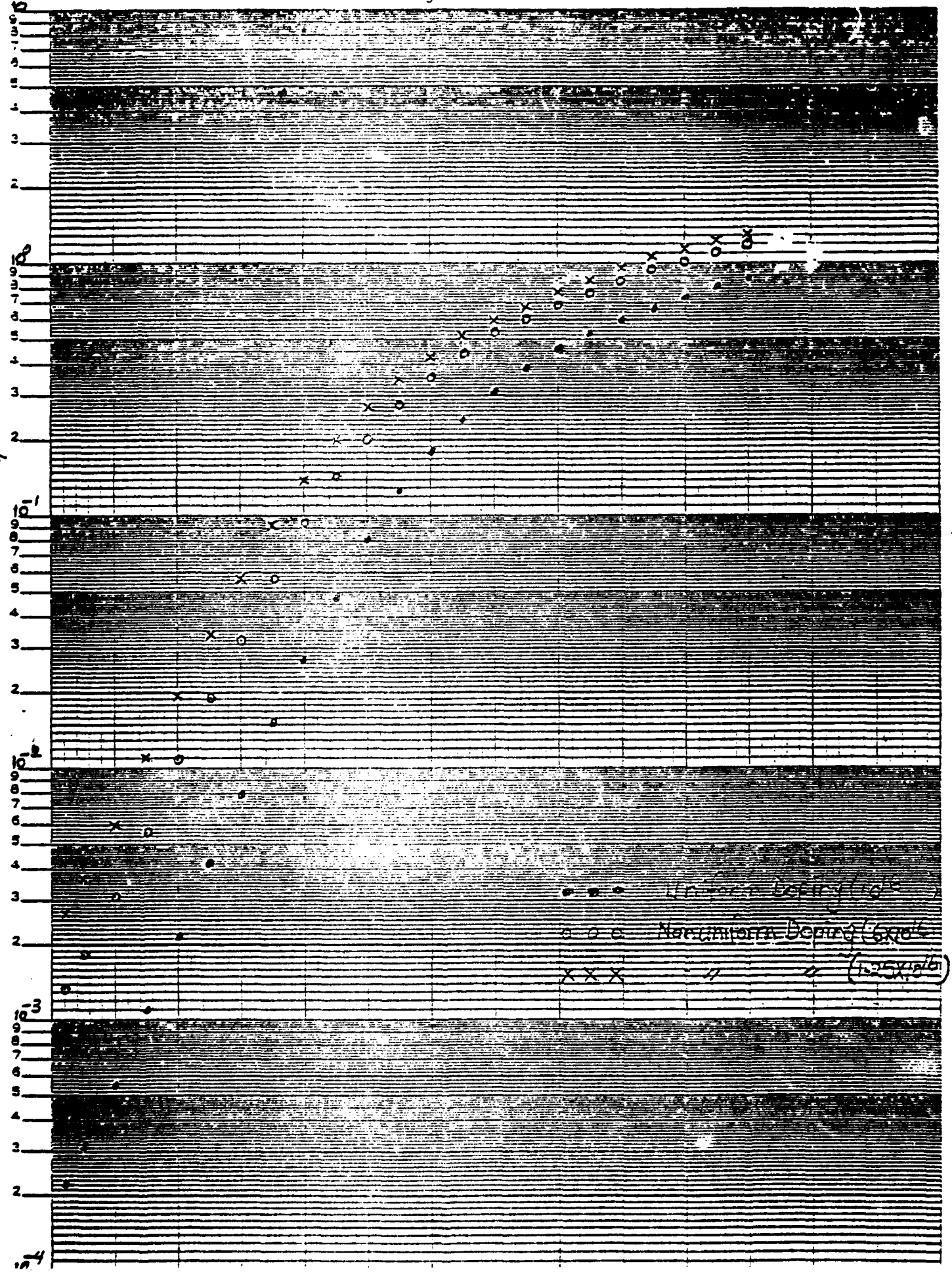
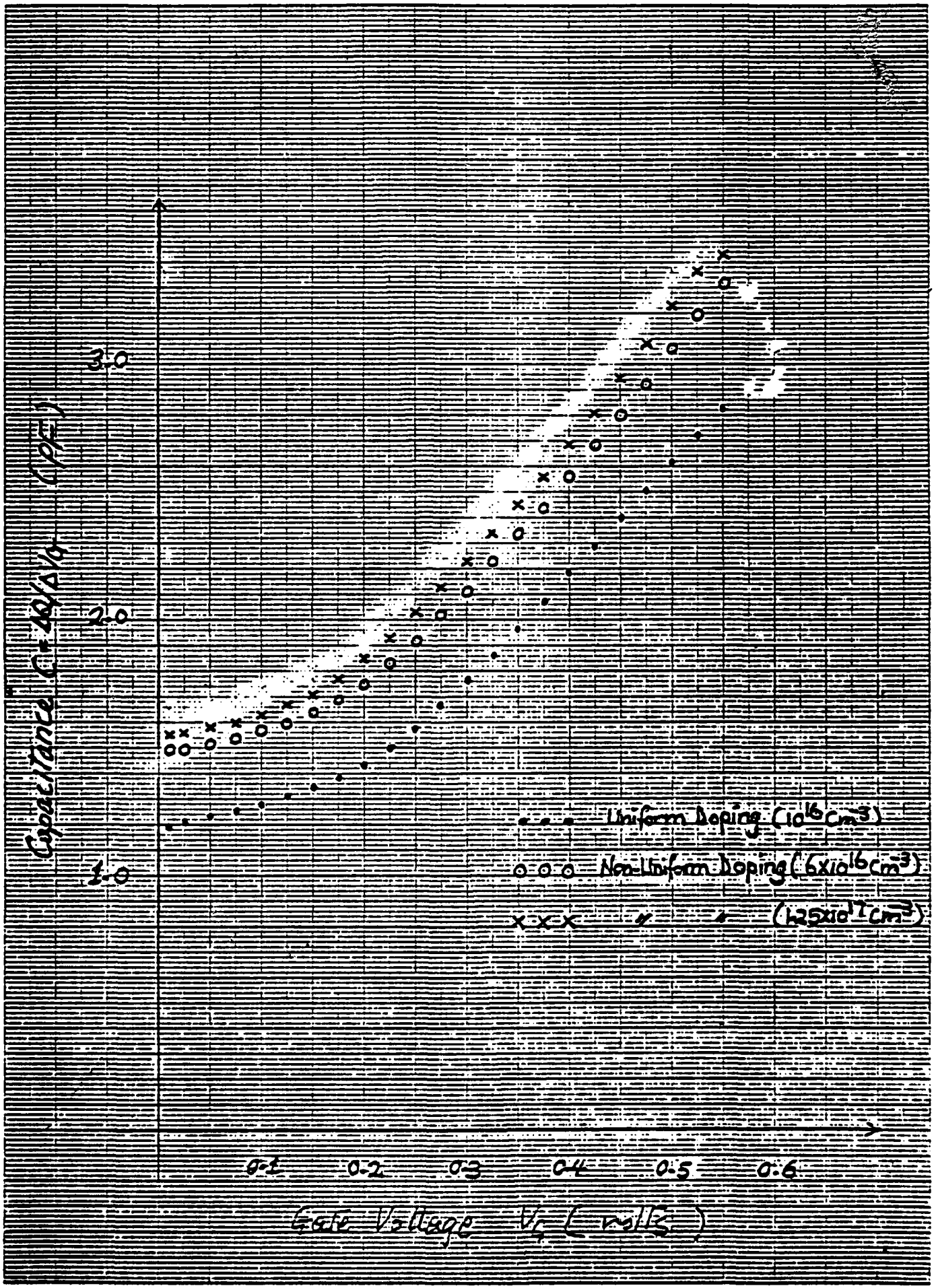

$g_m = \Delta I_D / \Delta V_G$
Uniform Doping (5x10^16)
Non-uniform Doping (5x10^16 - 1.25x10^16)

Figure 13


Capacitance C = ΔQ/ΔV (pF)
3.0
2.0
1.0
0.1
0.2
0.3
0.4
0.5
0.6
Gate Voltage V_G (volts)
Uniform Doping (10^{16} cm^{-3})
Non-Uniform Doping (6×10^{16} cm^{-3})
(1.25×10^{17} cm^{-3})

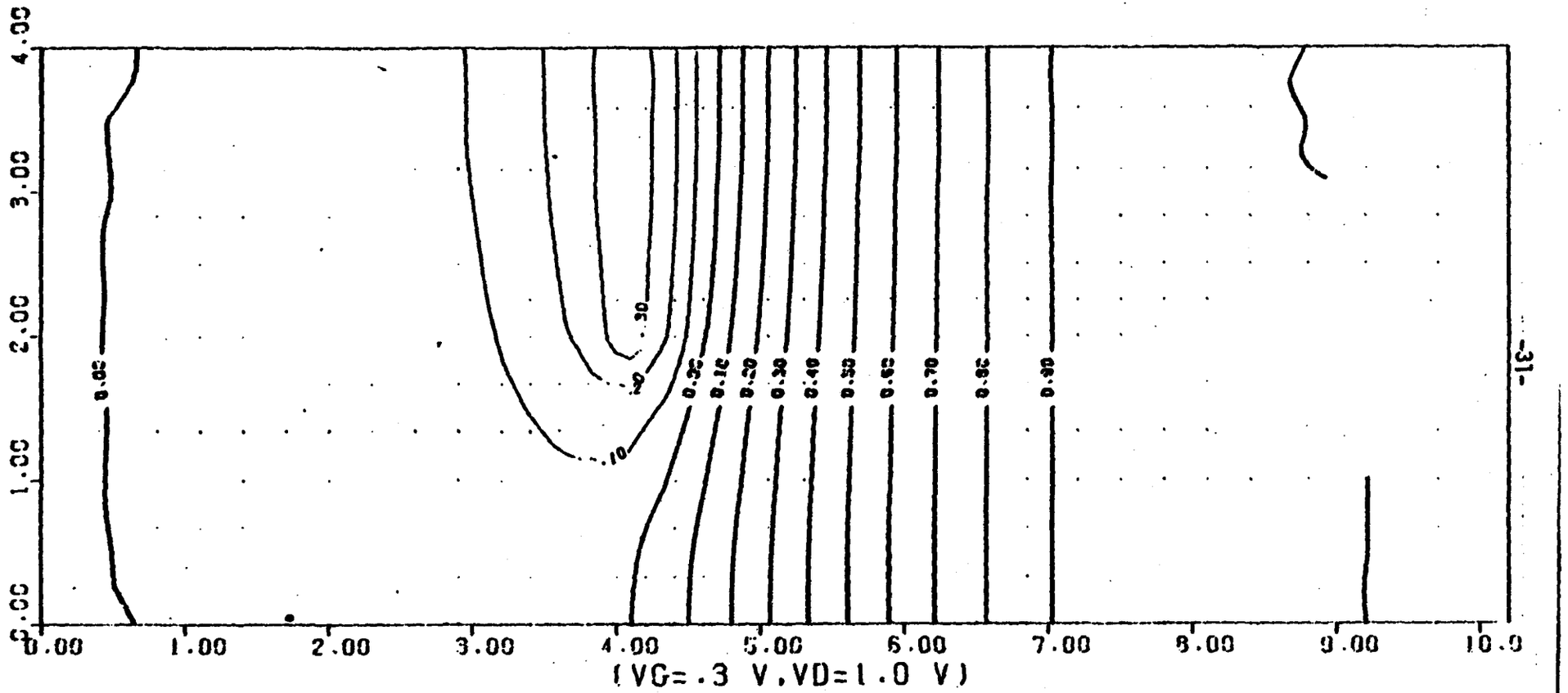

EQUIPOTENTIAL LINES (NU-6.E16)
4.00
3.00
2.00
1.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
7.00
8.00
9.00
10.0
(VG=.3 V,VD=1.0 V)

Figure 14

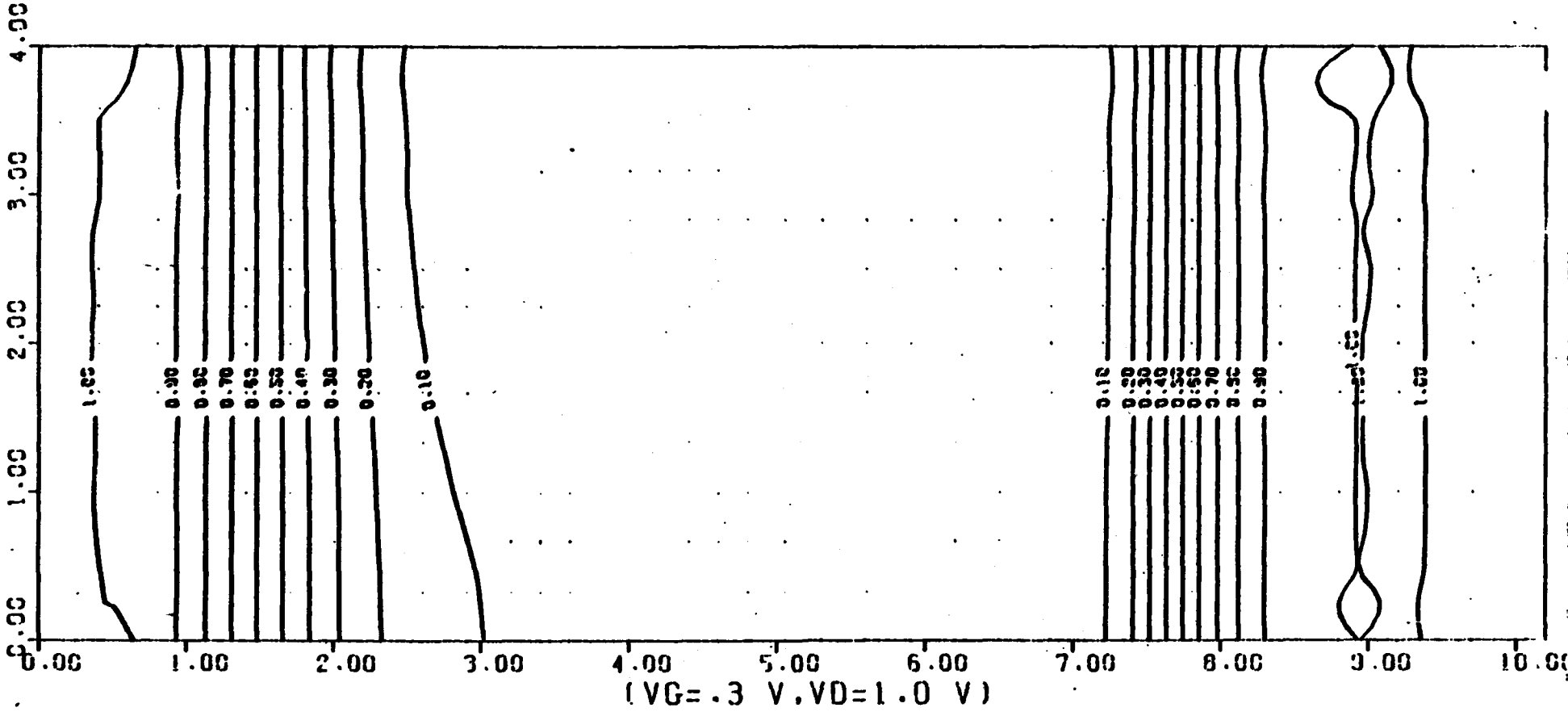

CONSTANT ELEC. DENSITY LINES (NU-6.E16)
4.00
3.00
2.00
1.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
7.00
8.00
9.00
10.00
(VG=.3 V,VD=1.0 V)

Figure 15

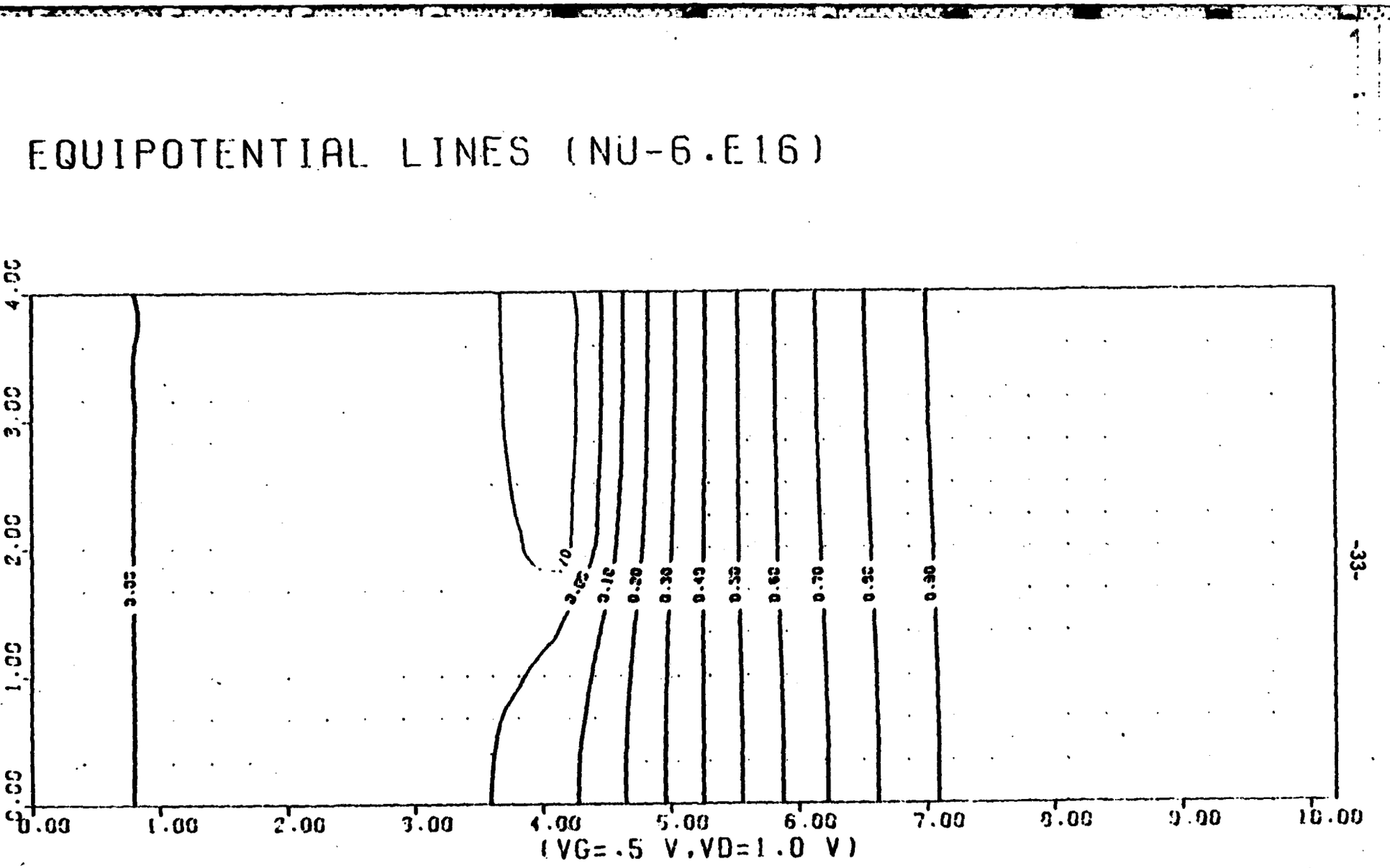

EQUIPOTENTIAL LINES (NU-6.E16)
4.00
3.00
2.00
1.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
7.00
8.00
9.00
10.00
(VG=.5 V,VD=1.0 V)

Figure 16

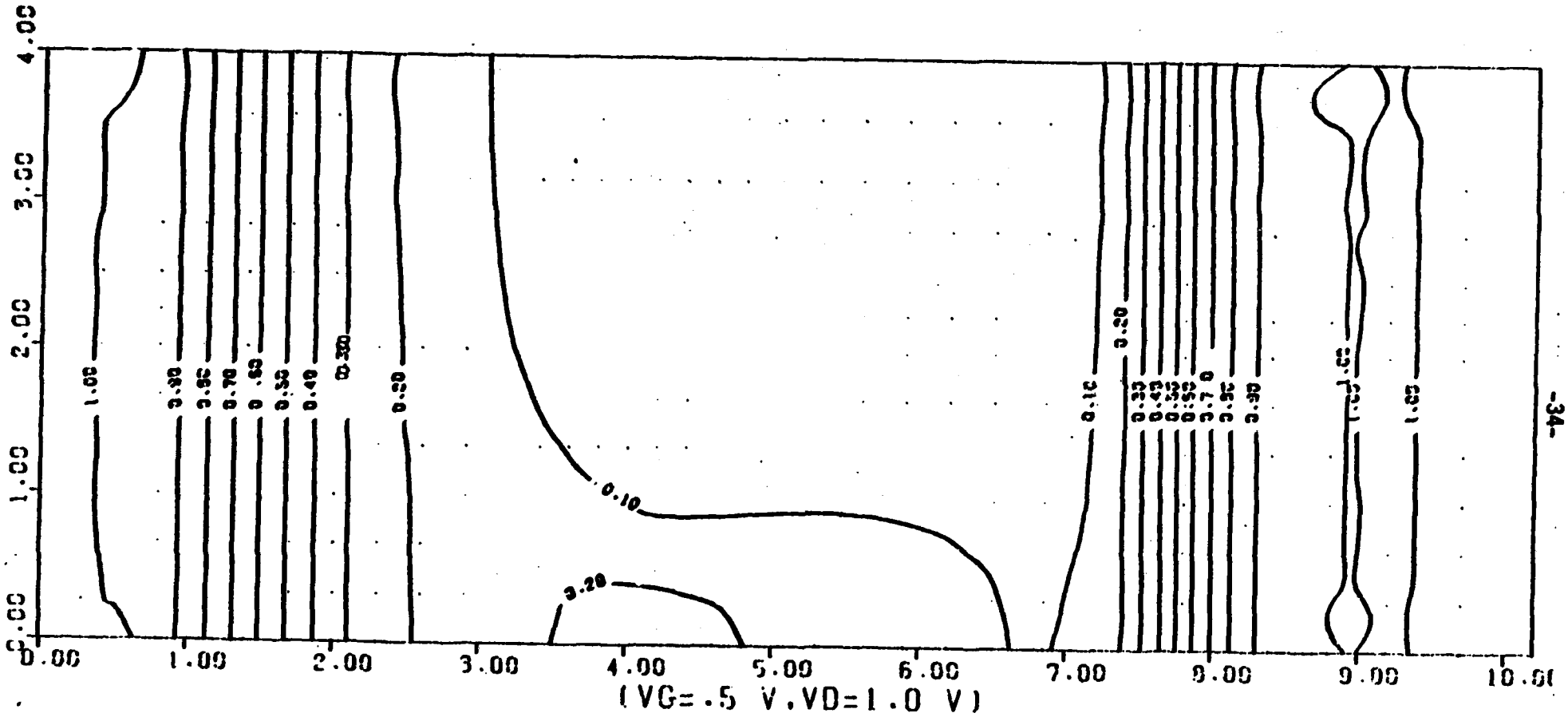

CONSTANT ELEC. DENSITY LINES (NU-6.E16)
4.00
3.00
2.00
1.00
0.00
0.10
0.20
0.00
1.00
2.00
3.00
4.00
5.00
6.00
7.00
8.00
9.00
10.00
(VG=.5 V,VD=1.0 V)

Figure 17

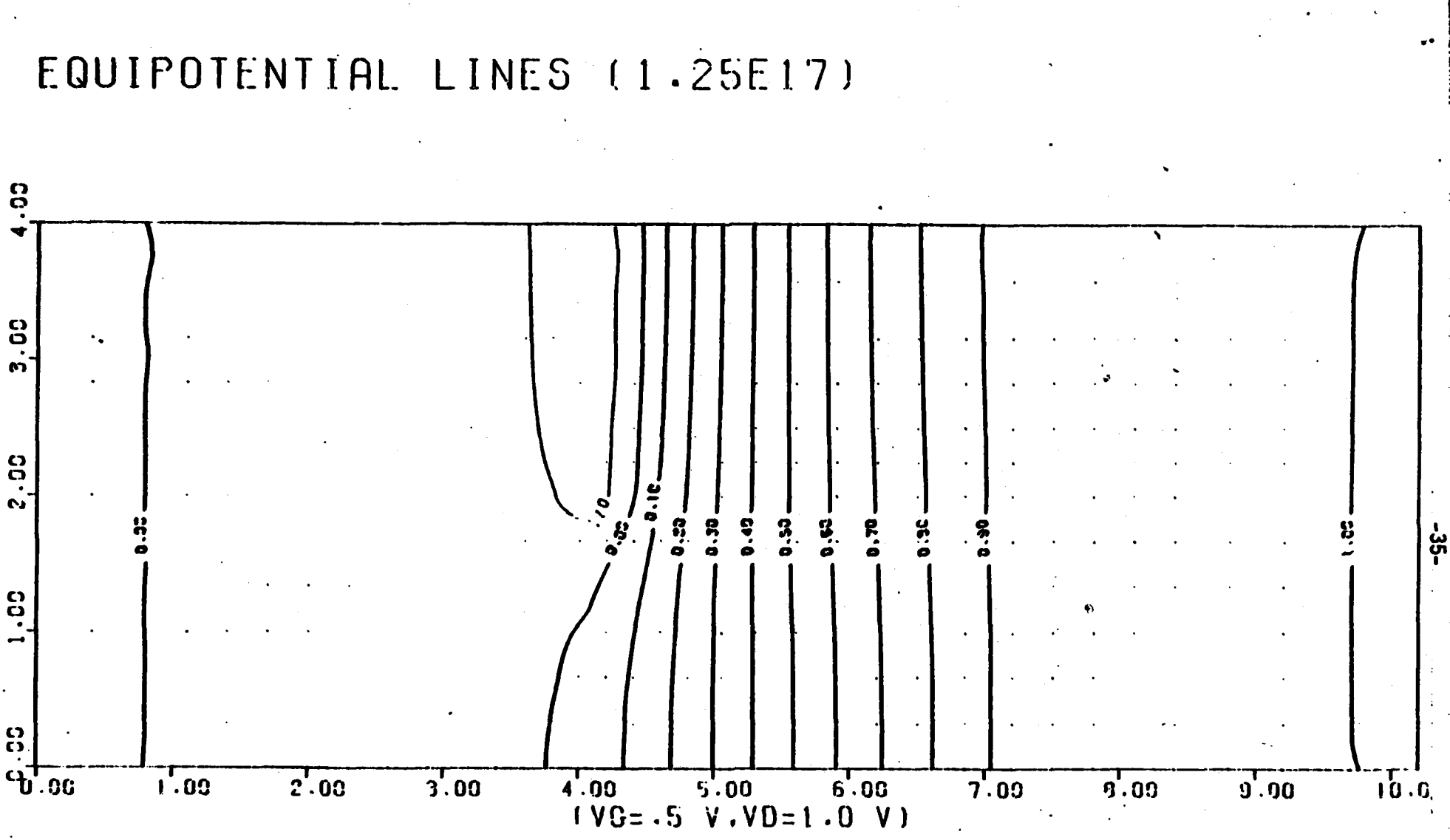

EQUIPOTENTIAL LINES (1.25E17)
4.00
3.00
2.00
1.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
7.00
8.00
9.00
10.0
(VG=.5 V,VD=1.0 V)
-35-

Figure 18

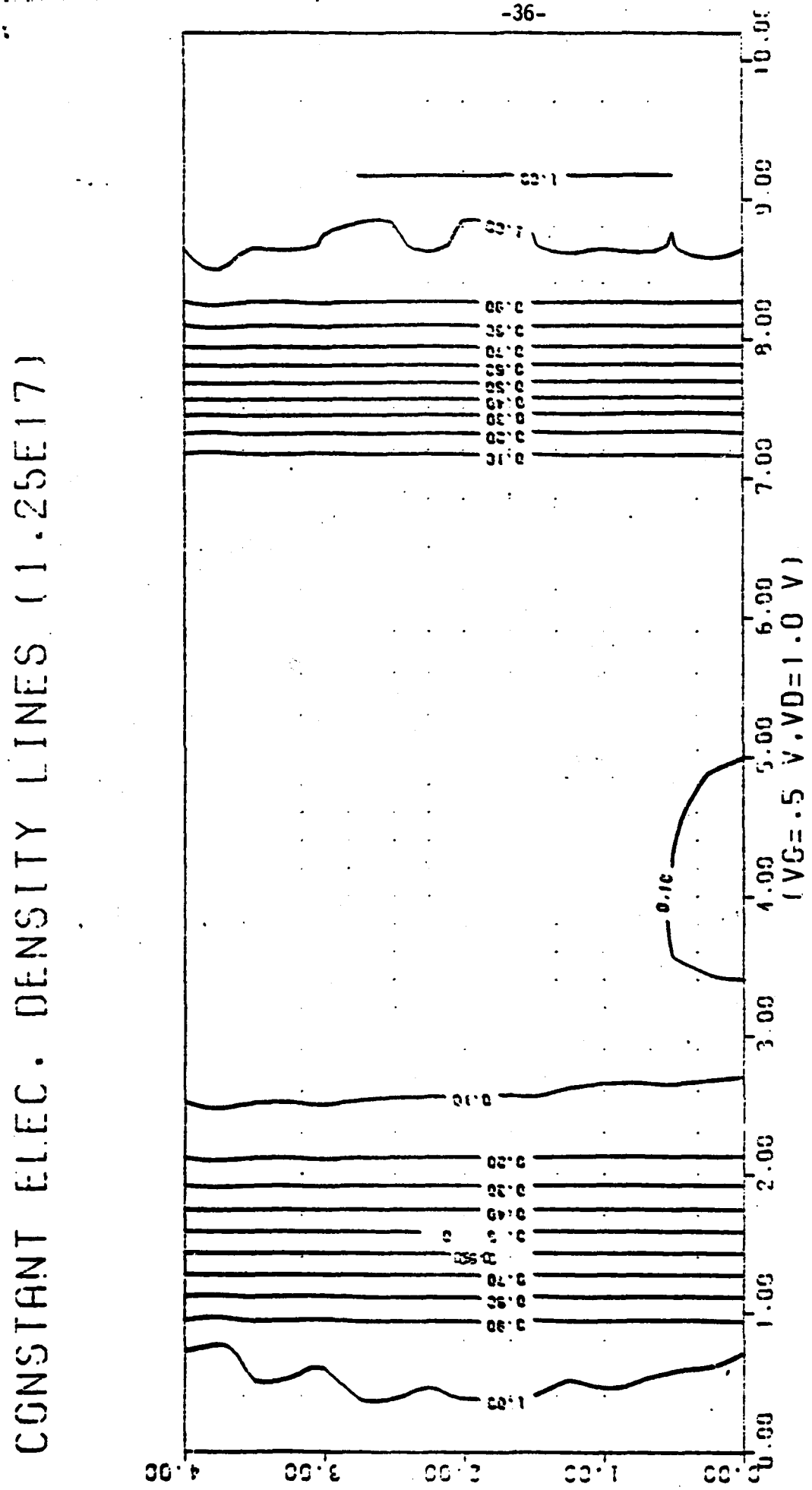

CONSTANT ELEC. DENSITY LINES (1.25E17)
(VG=.5 V, VD=1.0 V)
0.00
1.00
2.00
3.00
4.00
5.00
6.00
7.00
8.00
9.00
10.00

Figure 19

PBT WITH "TRENCH" ABOVE THE GATE REMOVED "Filled with Dielectric"

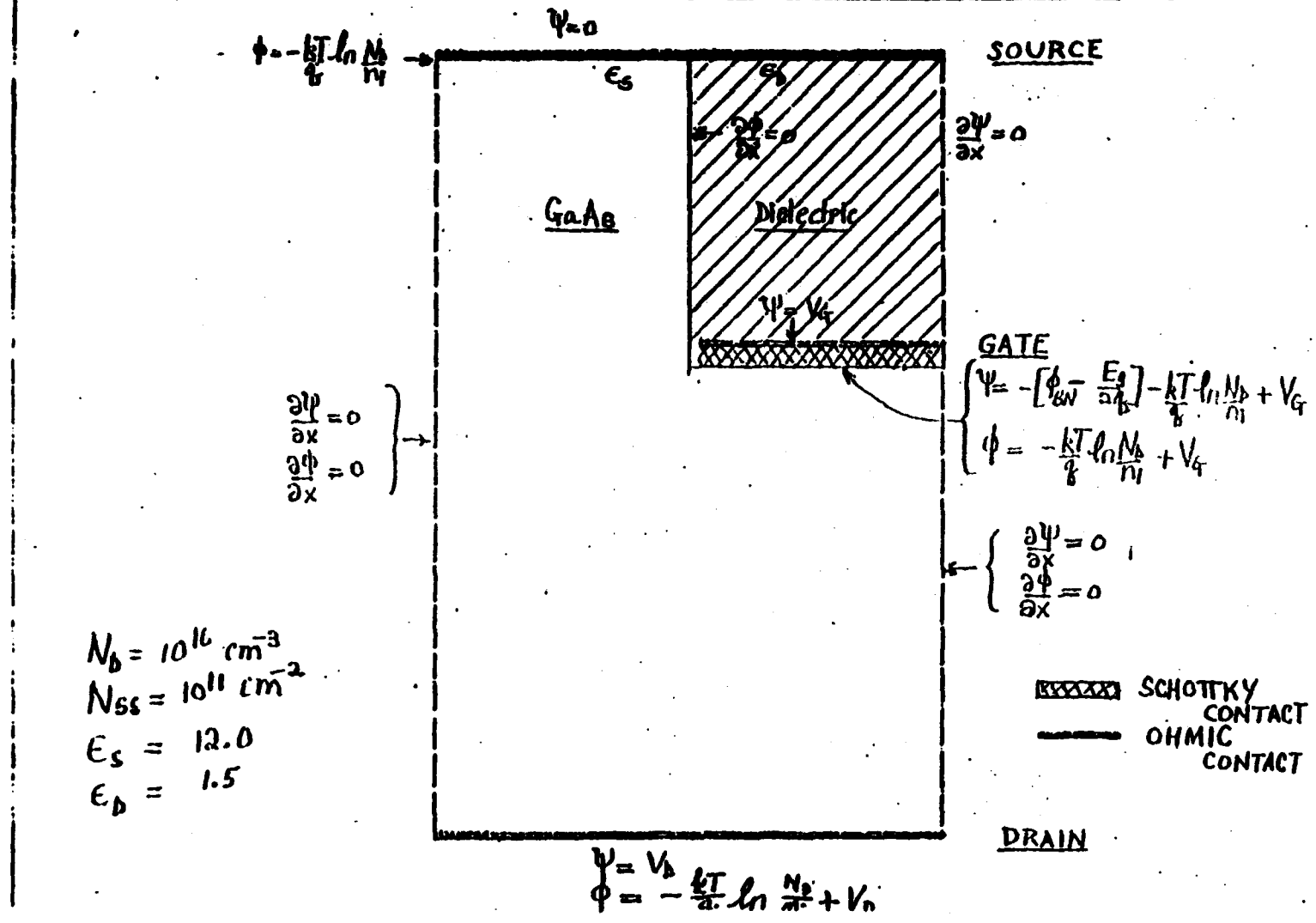


Figure 20

DRAIN CURRENT DENSITY (AMP CM⁻²)
P4
P3
P2
Qss = 0
PBT (Cm⁻² cm²)

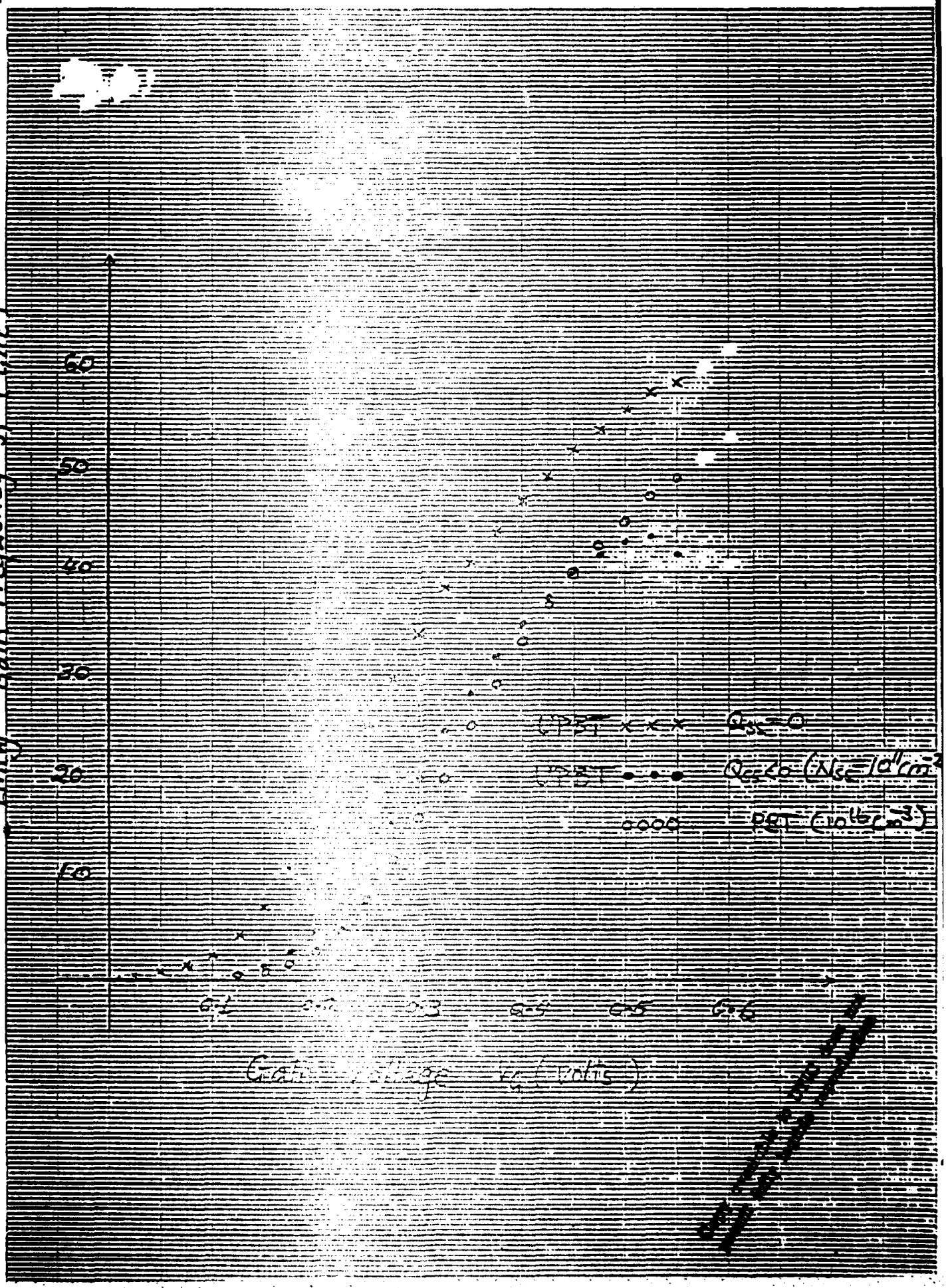
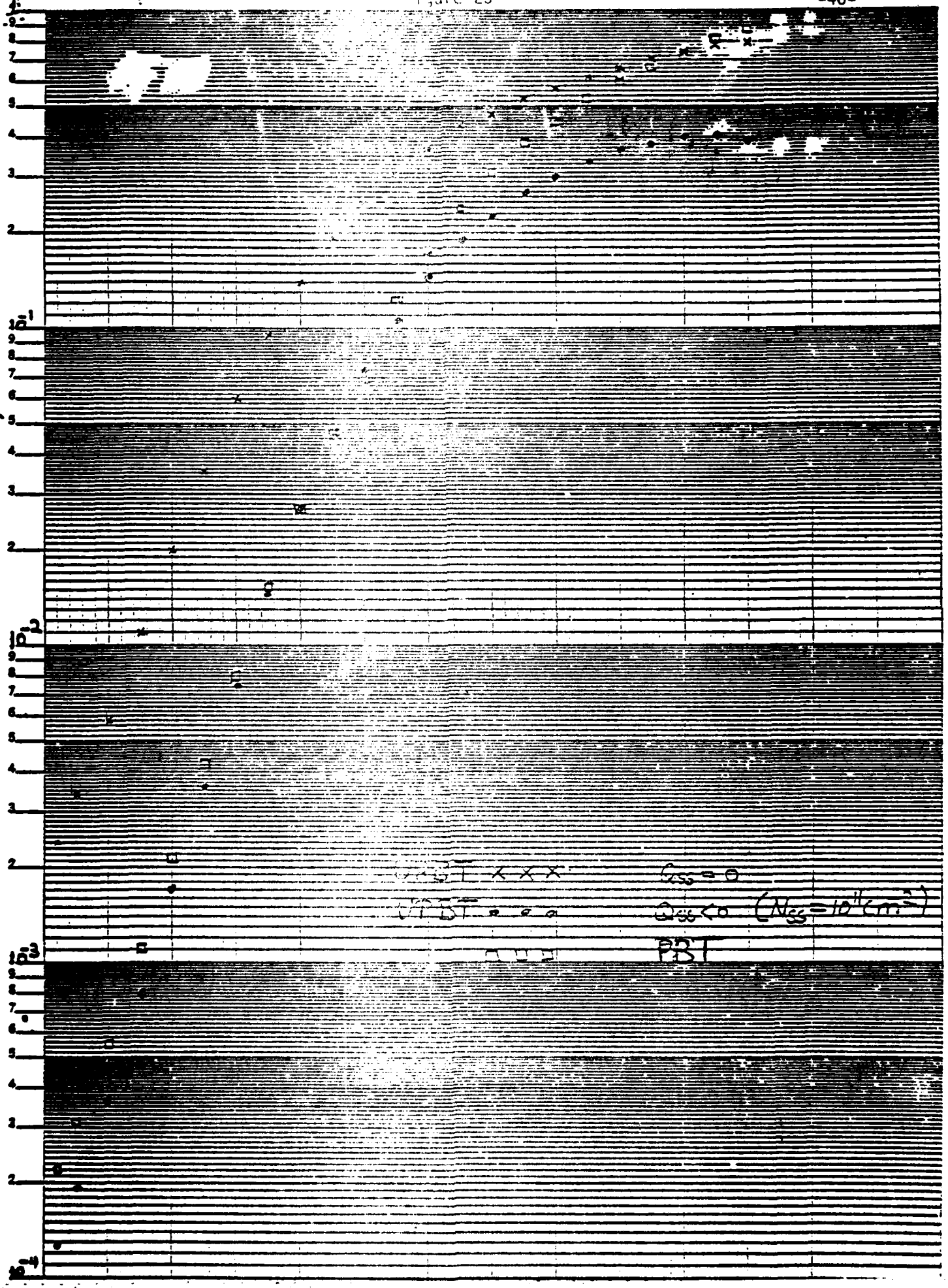
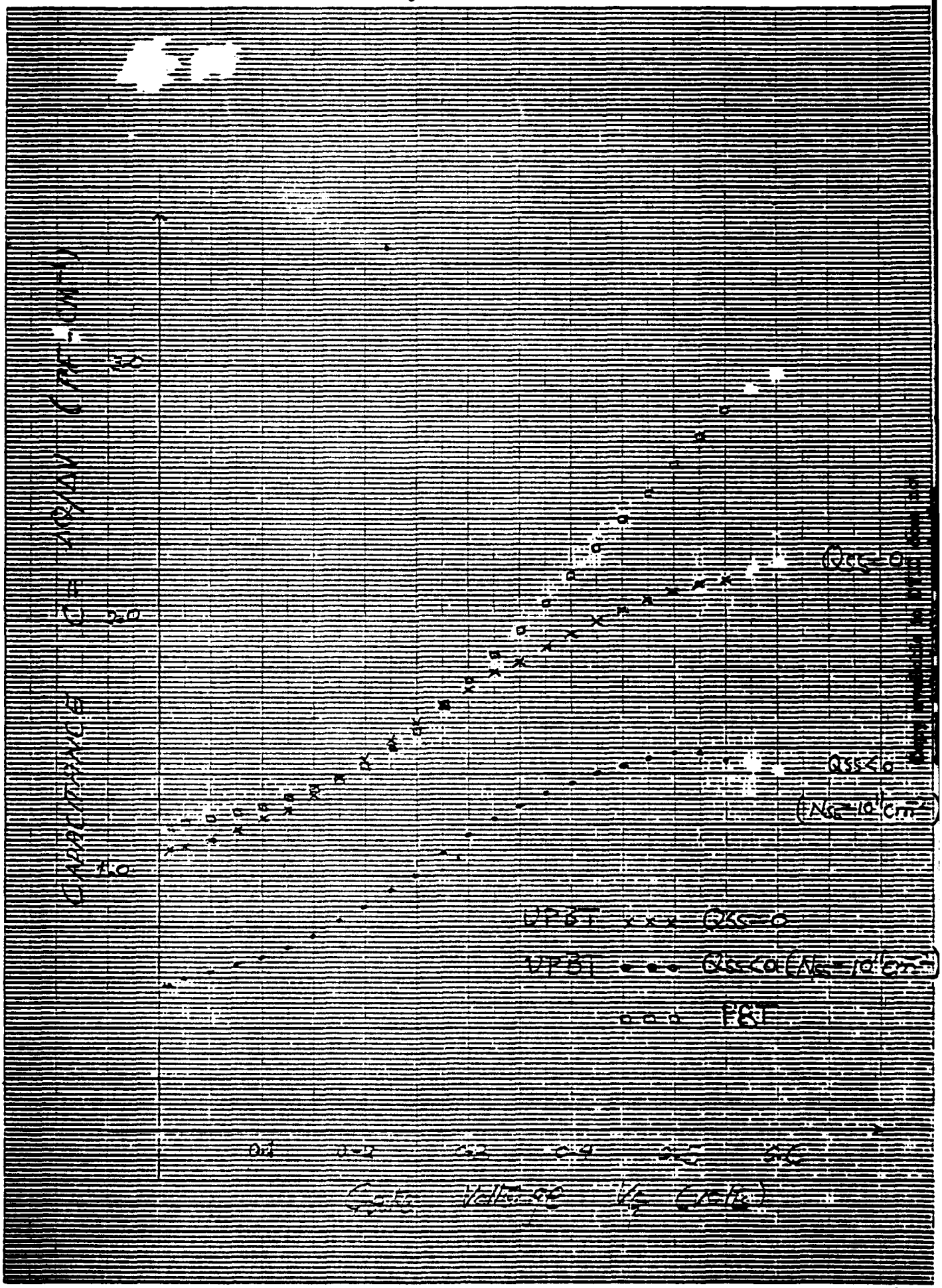

Unity Gain Frequency f_T (GHz)
60
50
40
30
20
10
UPBT
$Q_{ss}=0$
$Q_{ss}<0$ ($N_{ss}=10^{11}cm^{-2}$)
PBT ($10^{16}cm^{-3}$)
0.2
0.3
0.4
0.5
0.6
Gate Length L_g (Microns)

Figure 23




QSS=0
QSS<0
(NSS=10¹¹cm⁻²)
VFBT ××× QSS=0
VFBT ••• QSS<0 (NSS=10¹¹cm⁻²)
○○○ FBT

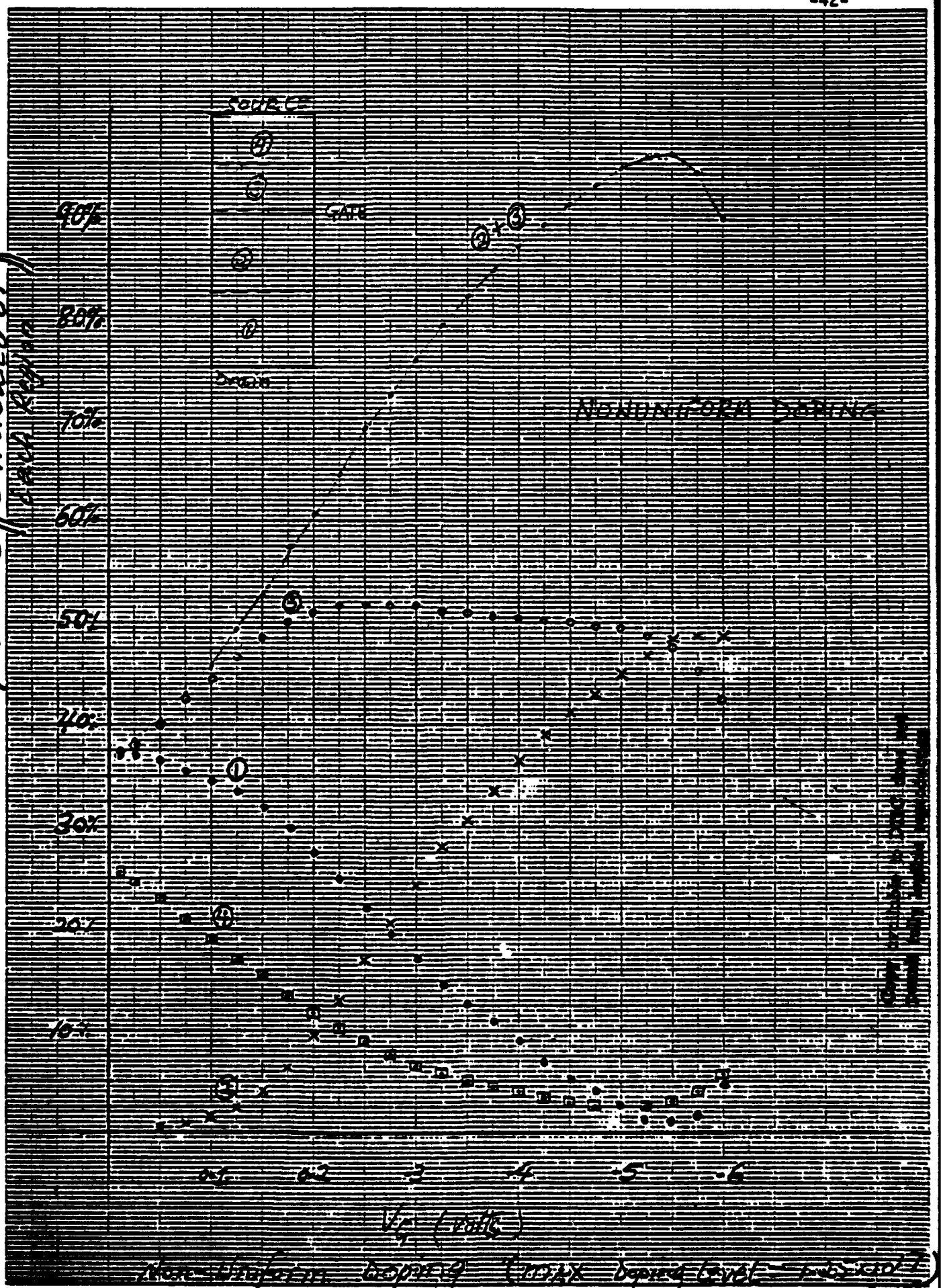

SOURCE
GATE
DRAIN
NONUNIFORM DOPING
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%
-2
-3
-4
-5
-6
% of Total Capacitance (Contributed by Each Region)
V_G (volts)
Note: Uniform doping (100% doping level = 5×10^16 cm^-3)

Figure 25

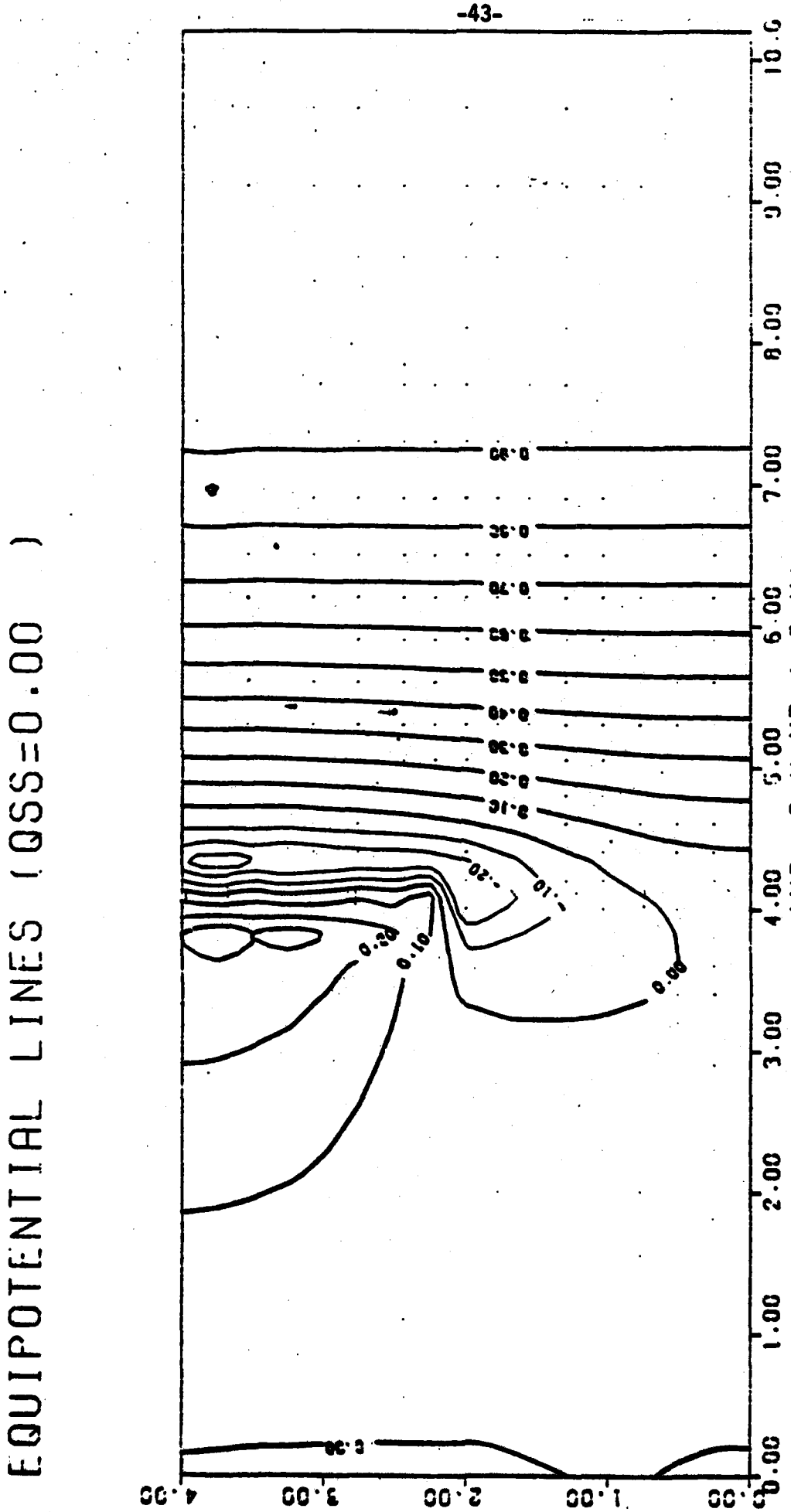

EQUIPOTENTIAL LINES (QSS=0.00)
(VG=-.3 V, VD=1.0 V)
0.00
1.00
2.00
3.00
4.00
5.00
6.00
7.00
8.00
9.00
10.0
0.00
1.00
2.00
3.00
4.00
0.90
0.80
0.70
0.60
0.50
0.40
0.30
0.20
0.10
0.00
-.10
-.20
-.30

Figure 26

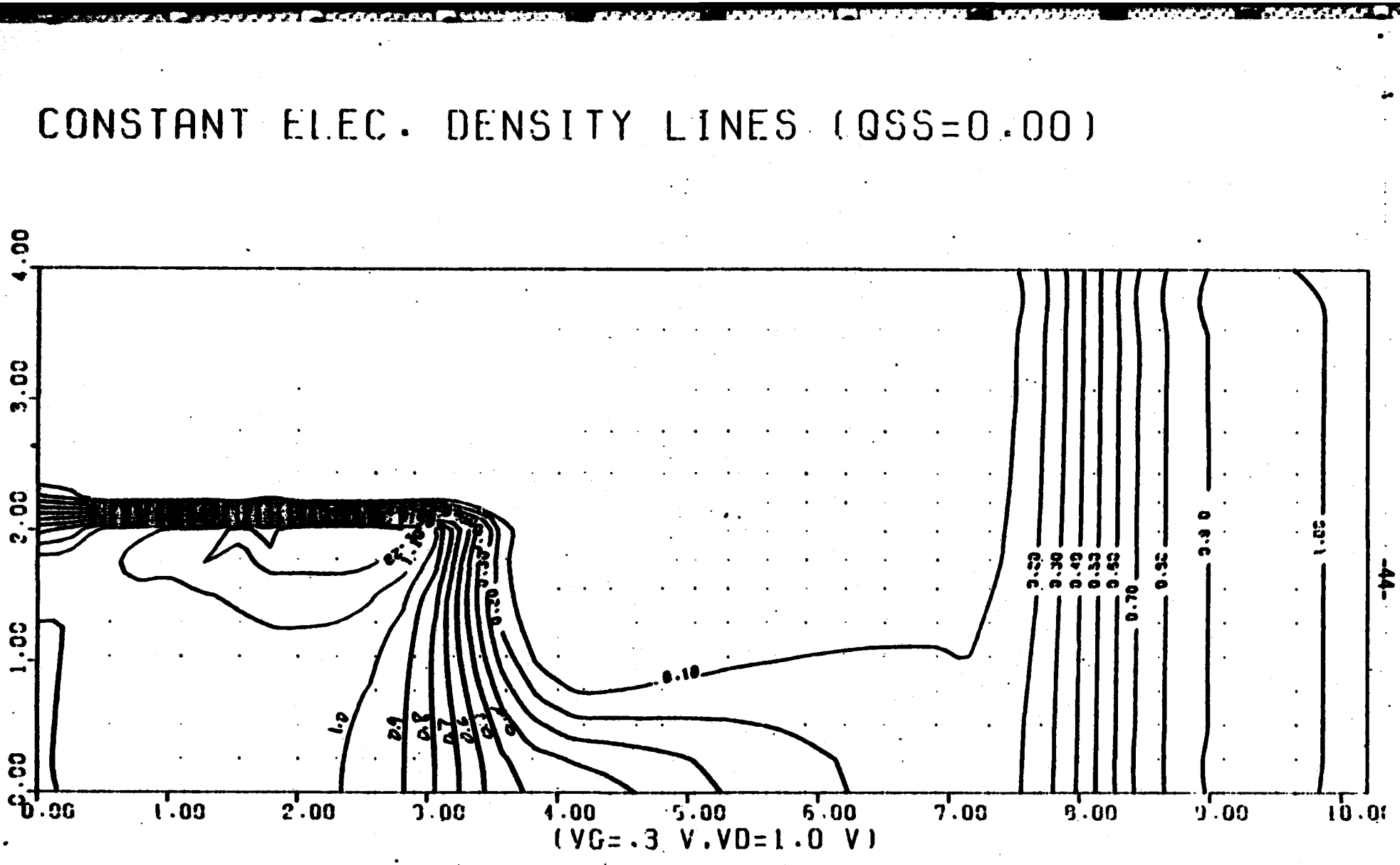

CONSTANT ELEC. DENSITY LINES (QSS=0.00)
4.00
3.00
2.00
1.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
7.00
8.00
9.00
10.00
0.10
0.30
0.50
0.70
0.90
1.10
(VG=.3 V,VD=1.0 V)

Figure 27

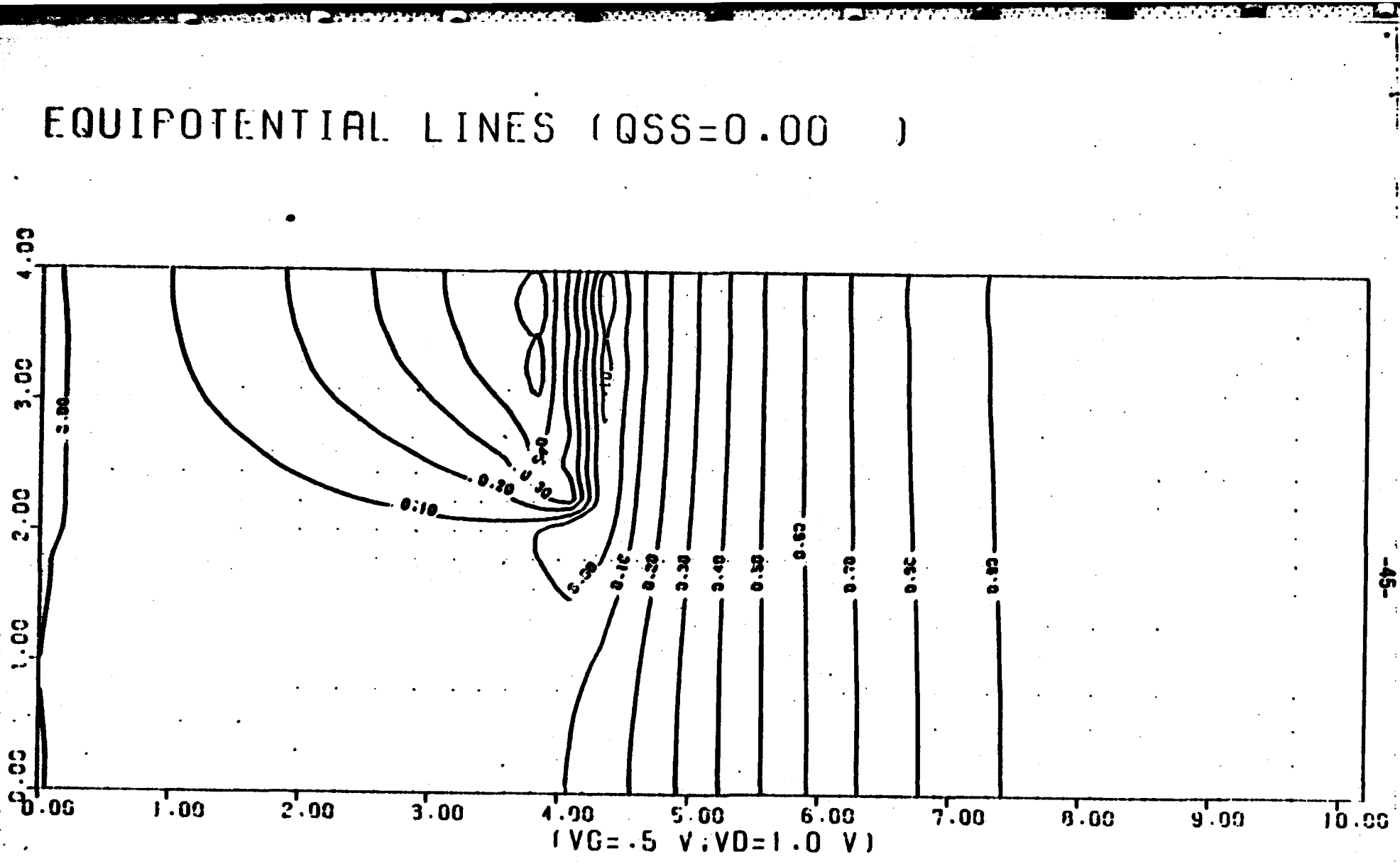

EQUIPOTENTIAL LINES (QSS=0.00)
4.00
3.00
2.00
1.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
7.00
8.00
9.00
10.00
(VG=.5 V;VD=1.0 V)

Figure 28

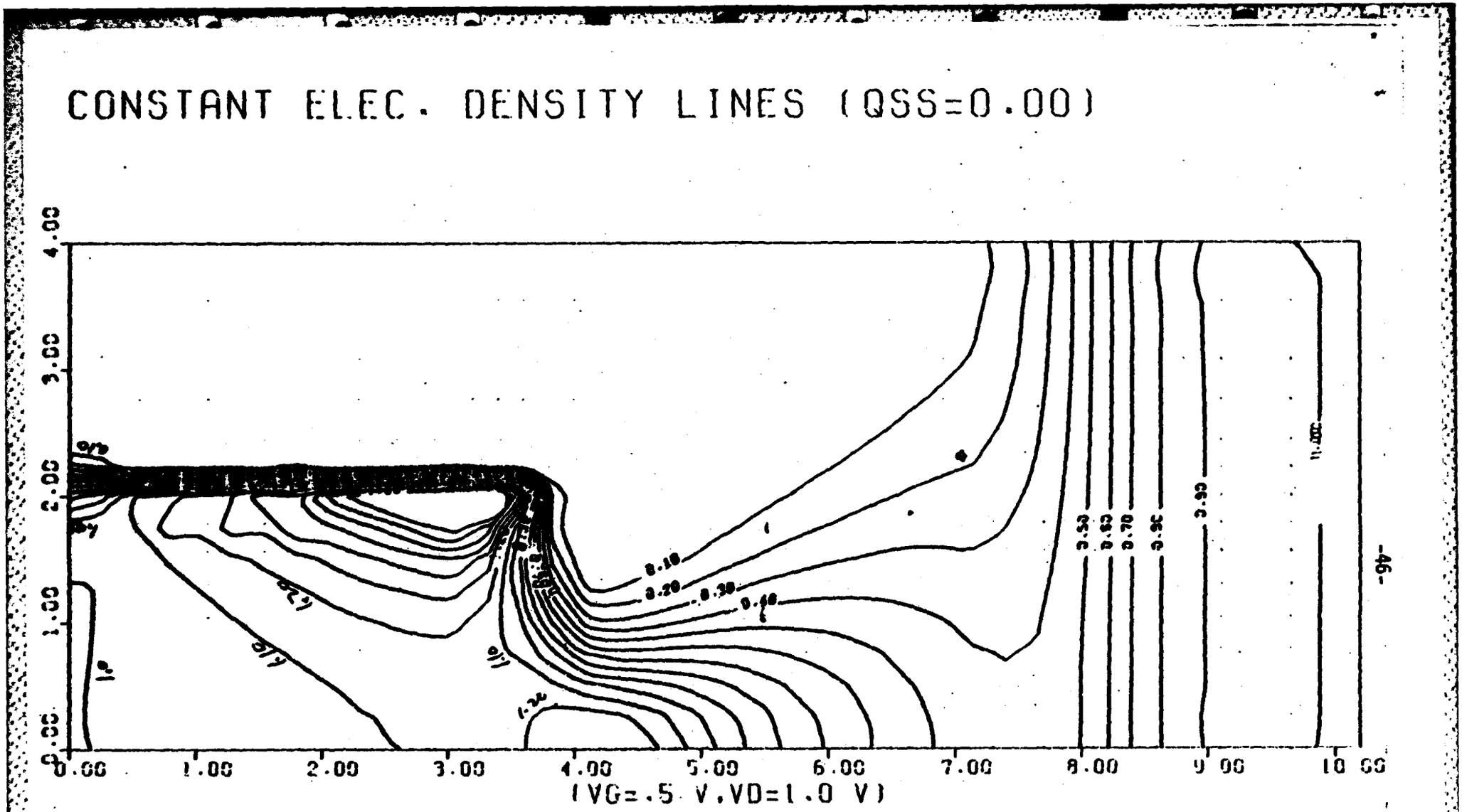

CONSTANT ELEC. DENSITY LINES (QSS=0.00)
4.00
3.00
2.00
1.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
7.00
8.00
9.00
10.00
(VG=.5 V,VD=1.0 V)
-46-

Figure 29

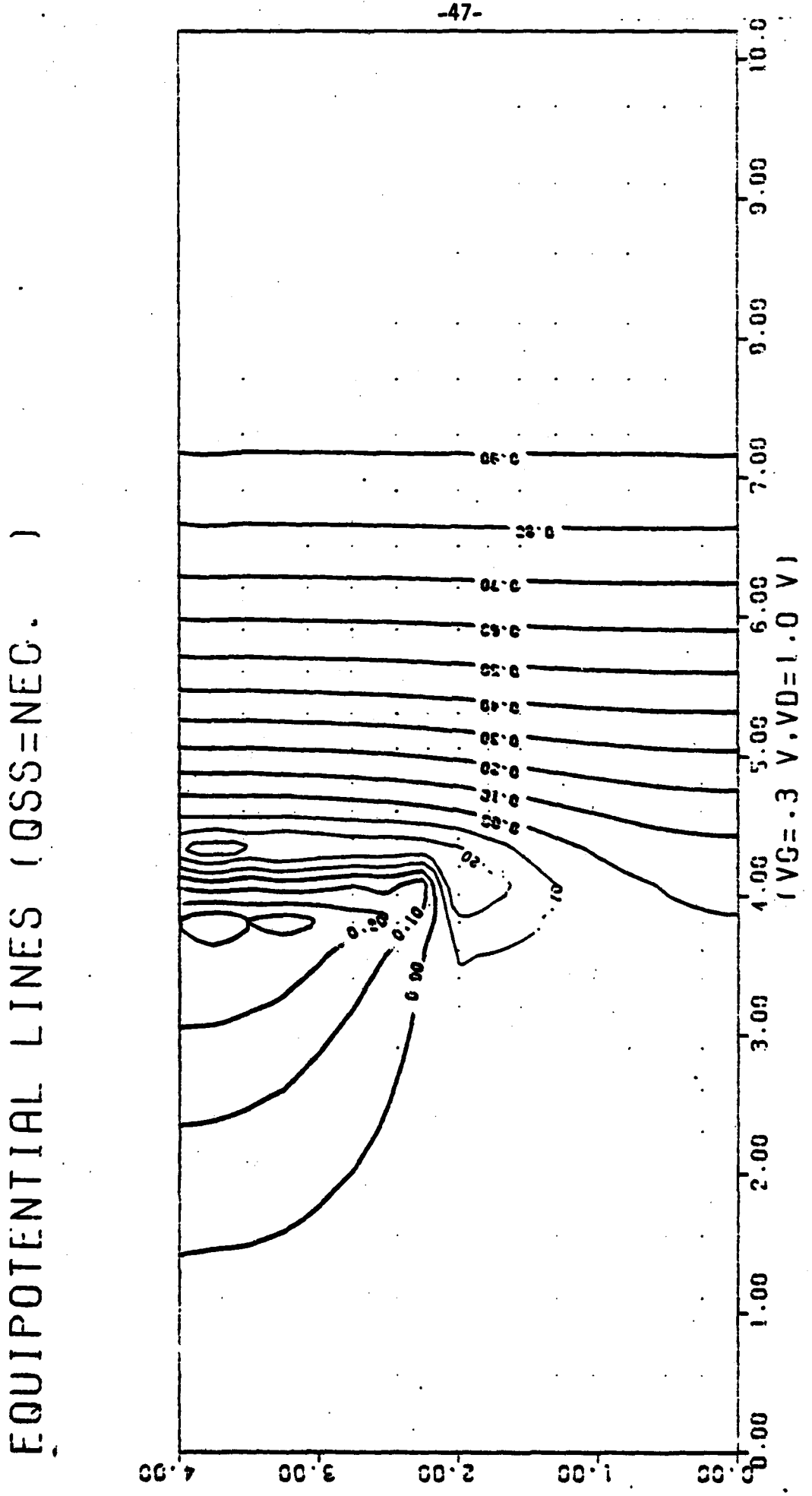

EQUIPOTENTIAL LINES (QSS=NEG.)
(VG=-.3 V, VD=1.0 V)
0.00
1.00
2.00
3.00
4.00
5.00
6.00
7.00
8.00
9.00
10.0
0.00
1.00
2.00
3.00
4.00
0.90
0.80
0.70
0.60
0.50
0.40
0.30
0.20
0.10
.02
.10

Figure 30

CONSTANT ELEC. DENSITY LINES (QSS=NEG.)

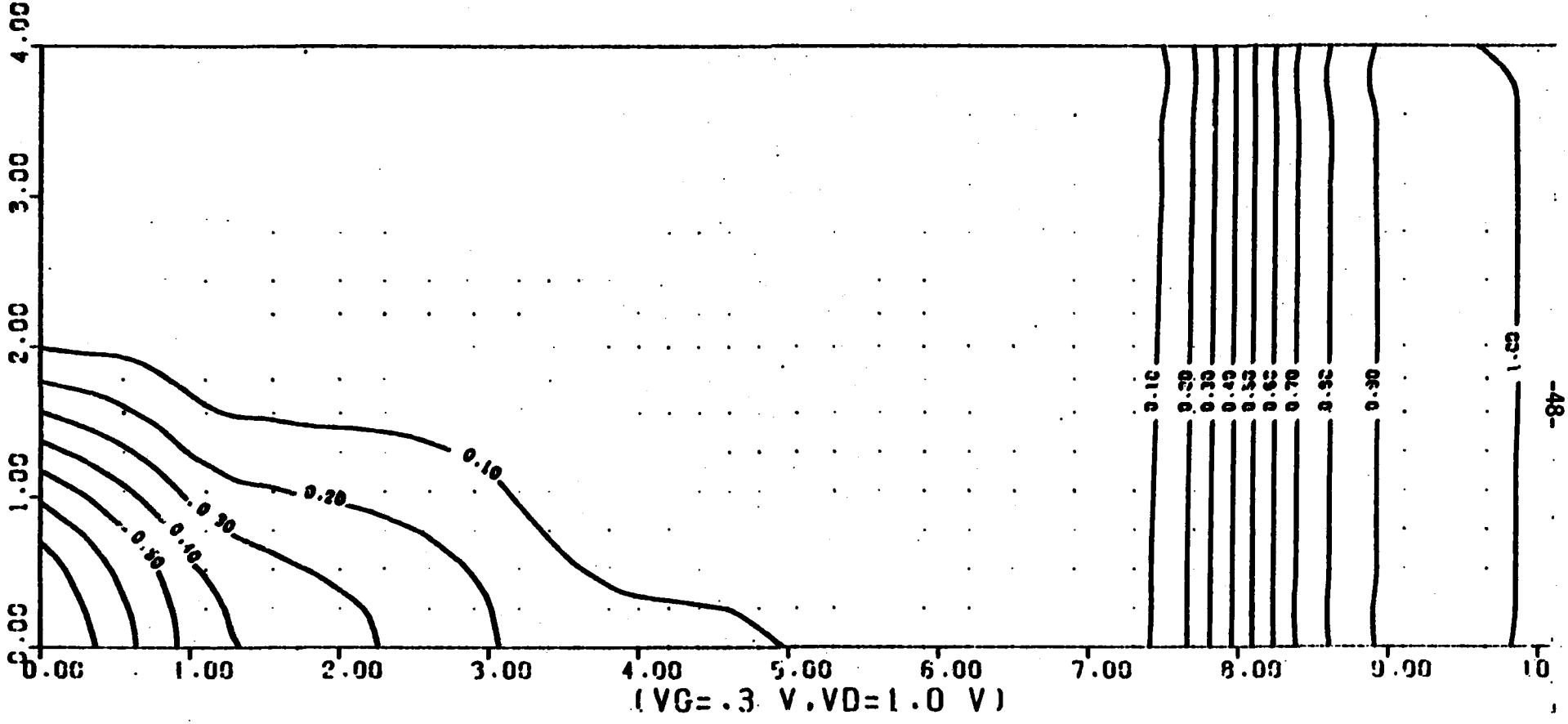


Figure 31

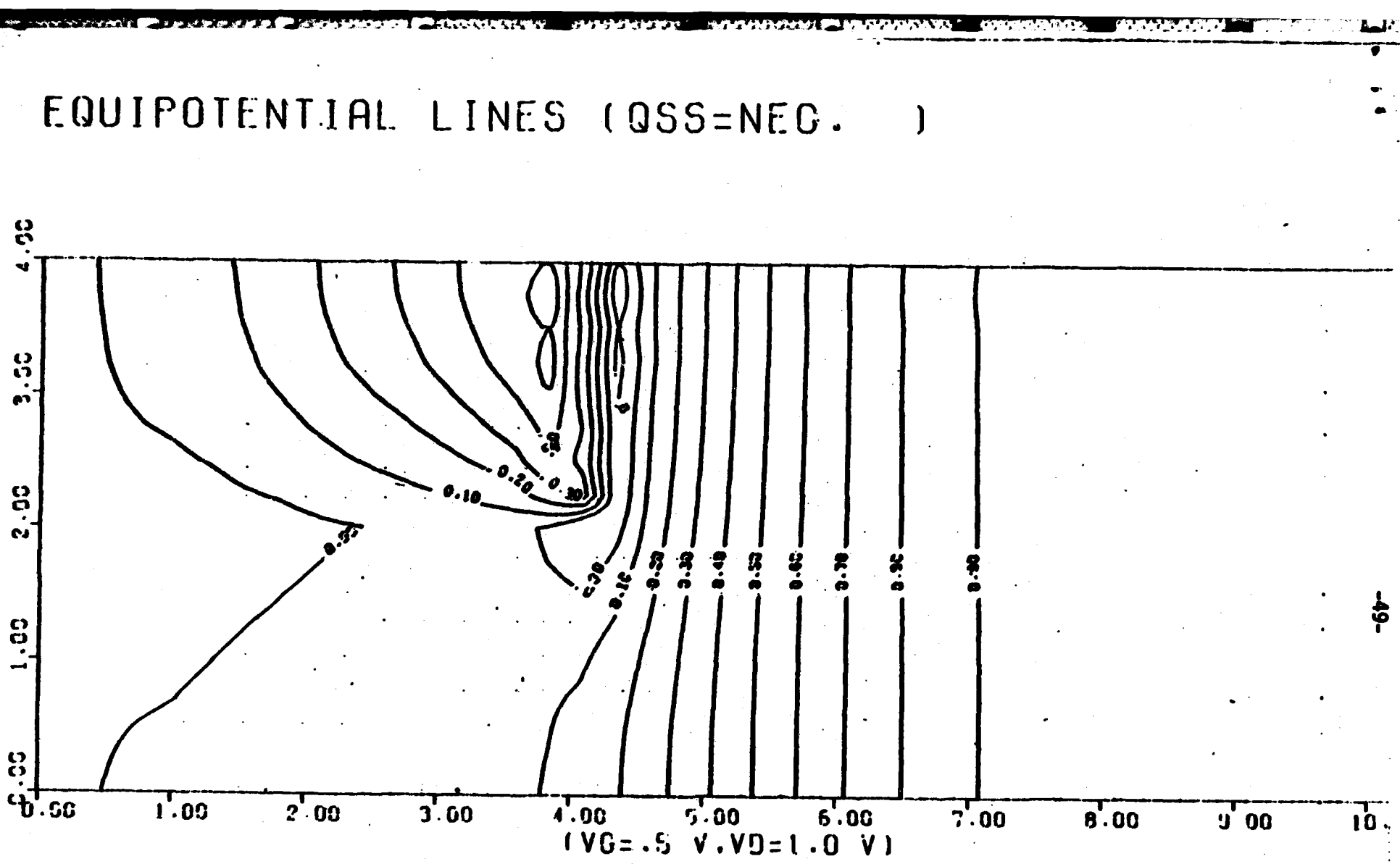

EQUIPOTENTIAL LINES (QSS=NEC.)
4.00
3.00
2.00
1.00
0.00
0.10
0.20
0.30
0.50
0.00
1.00
2.00
3.00
4.00
5.00
6.00
7.00
8.00
9.00
10.
(VG=.5 V,VD=1.0 V)

Figure 32

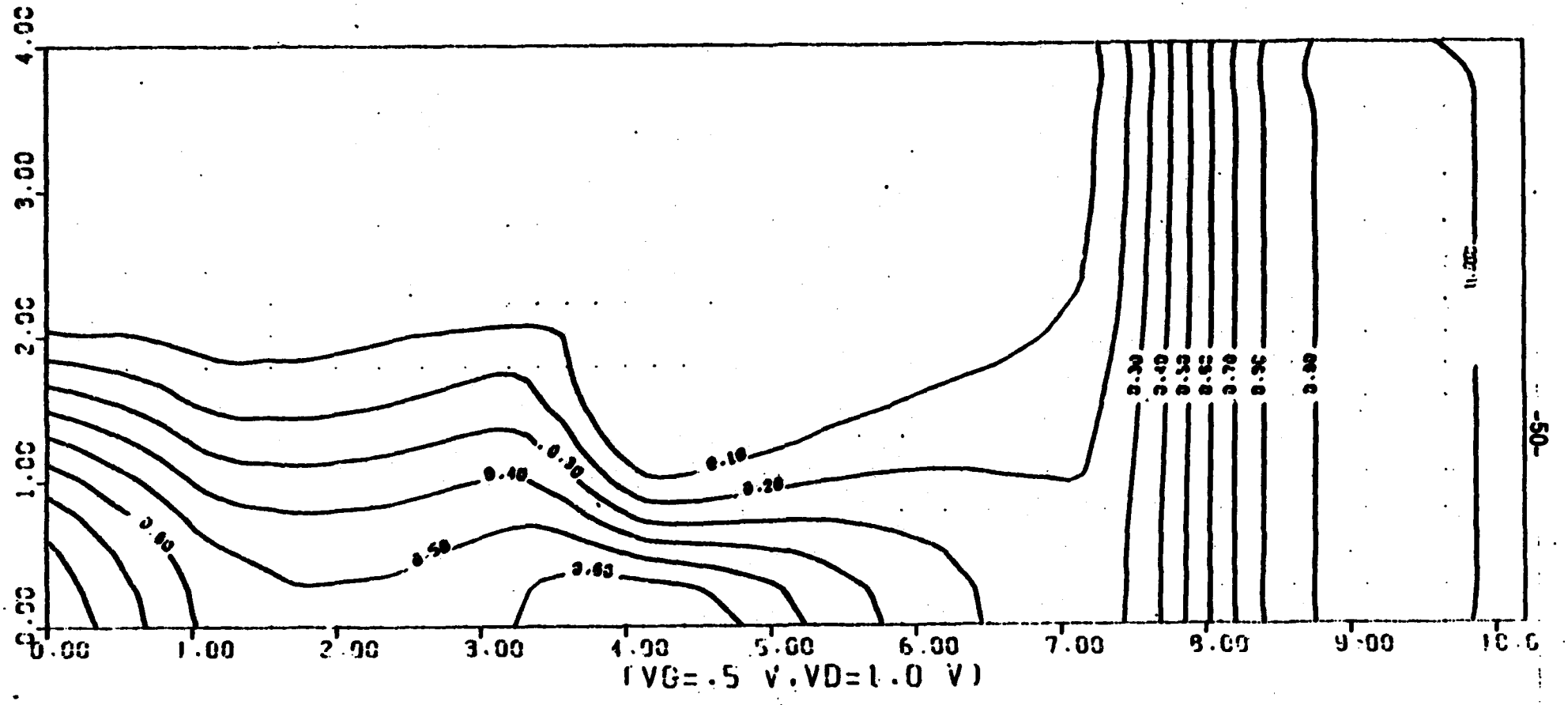

CONSTANT ELEC. DENSITY LINES (QSS=NEG.)
4.00
3.00
2.00
1.00
0.00
0.00
1.00
2.00
3.00
4.00
5.00
6.00
7.00
8.00
9.00
10.0
0.10
0.20
0.30
0.40
0.50
0.60
0.63
-50-
(VG=.5 V,VD=1.0 V)

Figure 33

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